12-BIT HIGH SPEED DIRECT DIGITAL FREQUENCY SYNTHESIZER BASED ON PIPELINING PHASE ACCUMULATOR DESIGN

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ABSTRACT

This paper presents high speed direct digital frequency synthesizer (DDFS) based on pipelining phase accumulator (PA). The proposed 12-bit PA contains three pipelining stages with 4-bit carry-lookahead adder (CLA) with the carries ripple between these stages. Comparing results between similar phase accumulator designed with ripple carry adder on, Cyclone III FPGA platform reveals that the proposed phase accumulator runs approximately 10.5% and 13% faster than conventional phase accumulator in approximately for 12-bit and 18-bit respectively.

Key Words: Direct digital frequency synthesizer (DDFS), Carry-lookahead adder (CLA), Ripple carry adder (RCA)

INTRODUCTION

Direct digital frequency synthesizer (DDFS) or direct digital synthesizer (DDS) is a technique to generate frequency output signal referenced to a fixed-frequency precision clock source (E. Murphy 2004). Nowadays DDFS became a preferred candidate for radars and communication systems due to its interesting features such as high speed, high frequency resolution, and fast frequency channels switching. In DDFS, all of the signal-processing operations that synthesize the sine wave are performed digitally (Ching-Yuan, Jun-Hong et al. 2011). The pipeline technique has been widely used to achieve higher speed phase accumulator (Chappell and McEwan 2004; Jensen, Khafaji et al. 2012). In (Xueyang, Dai et al. 2010), eleven stages with 1-bit full adder was used to design 11-bit PA. Large numbers of DFF used in PA lead to high power consumptions. Standard

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DDFS consist of the phase accumulator (PA), sine or cosine look-up-table (LUT) to convert the phase to amplitude signals, digital to analog converter (DAC) in which the amplitude sine wave signals are converted into analog signal waves and the low pass filter (LPF) to remove the unwanted harmonic pulses of the output signals. The block diagram of the DDFS is shown in figure 1.

Figure-1. Block diagram of Direct Digital Frequency Synthesizer
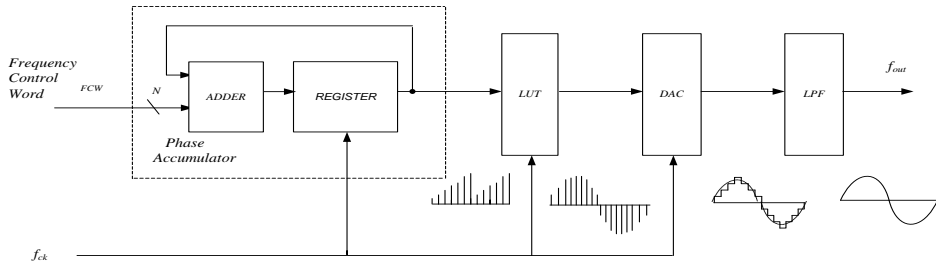
The output frequency (f_{out}) of the DDFS can be calculated based on equation (1)

$$f_{out} = \frac{FCW}{2^N} \times f_{clk} \qquad \text{(McCune 2010)} \qquad (1)$$

Where f_{out} –the output frequency, *FCW* – frequency control word , f_{clk} – clock frequency and *N* - bit-input number.

The pipelining technique is commonly used to increase the speed by dividing into a number of subtasks (Mostafa Abd-El-Barr 2004). The proposed architecture consists of a number of stages with 4-bit CLA adder and 4-bit register in each of the stages. In this paper we present a high speed 12-bit DDFS using pipeline PA design, with 4-bit CLA adder in each of the pipeline stages, the carries are rippled between the stages.

12-BIT PHASE ACCUMULATOR DESIGN

The block diagram of the proposed PA is shown in figure 2.

Figure-2. Block diagram of 12-bit phase accumulator.
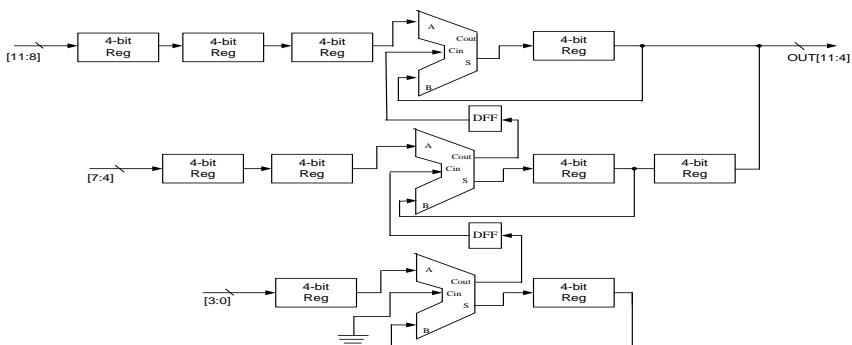
Carry Look-ahead Adder Design

High speed operation is one of the important requirements in a DDFS system.. The phase accumulator (PA) is a key element of the DDFS system and the adder is the core of the PA. Therefore, the improvement of the adder design can lead to the increasing speed of the phase accumulator hence the DDFS.

The carry out of the adder can be quickly determined if the carry-in from the previous stage have a value 0 or 1 in each stage (Brown 2005), The carry-out functions of n stages can be derived from equation (2).

$$C_{n+1} = g_n + p_n C_n \qquad (2)$$

Where

$$g_n = x_n.y_n$$

$P_n = x_n \oplus y_n$

g_n , P_n- generate and propagate function.

n - bit number

Therefore the carry-out functions of one stage is:

$$C_1 = g_1 + p_0 C_0 \qquad (3)$$

For the other stages can be writing the following equation:

$C_n =$
$g_n + p_n. g_{n-1} + p_n.p_{n-1}g_{n-2} + - - - \quad - - - g_0 + \qquad p_n.p_{n-1} .p_{n-2} - - - - p_0 C_0 (4)$

The critical path for CLA adder is three gate delays (one gate for p, g input and two AND-OR gate), regardless of the number of input bits, as shown in Figure 3(a). Figure 3(b) shows the critical path for RCA adder which passes through the x, y input (first gate) and ripple sequentially through the circuit with two gate delays for each bit. Therefore the total gate delays along the critical path for RCA adder is (2n+1). (Salah H. 2011).

**Figure-3.** The critical path for CLA and RCA adder
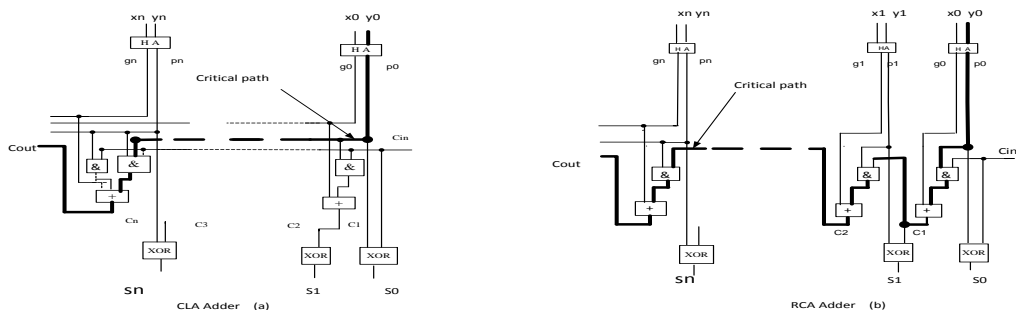
IMPLEMENTATION OF 12-BIT PHASE ACCUMULATOR DESIGN

We have designed and compiled the 12-bit pipelining PA using Verilog Hardware Description Language targeting for Cyclone III FPGA kit. The Register Transfer Level (RTL) and gate level simulation plot of the 12-bit PA is shown in figures 4 and 5.:

Figure-4. The Register Transfer Level (RTL) viewer of the 12-bit PA
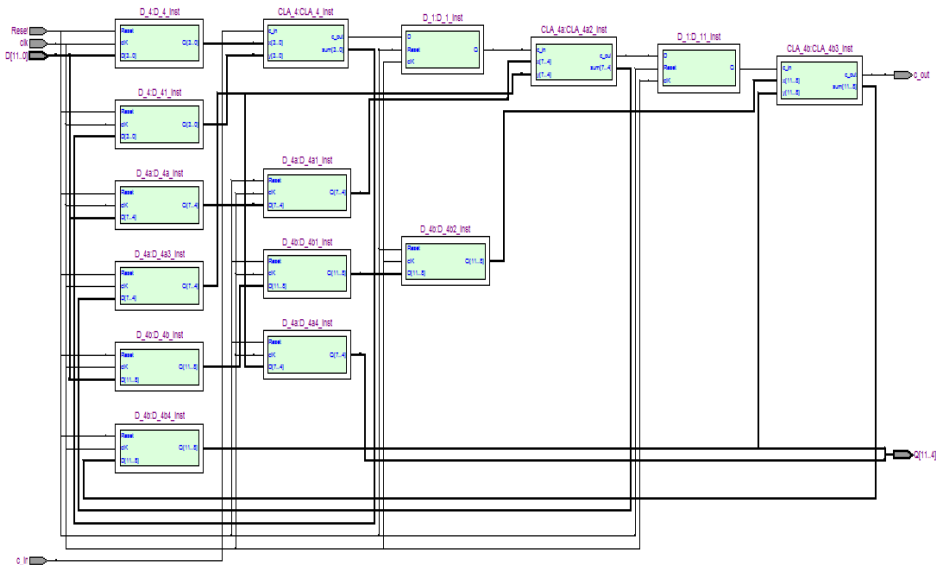
Figure-5. the phase accumulator (PA) and Lookup table (LUT) gate level simulation
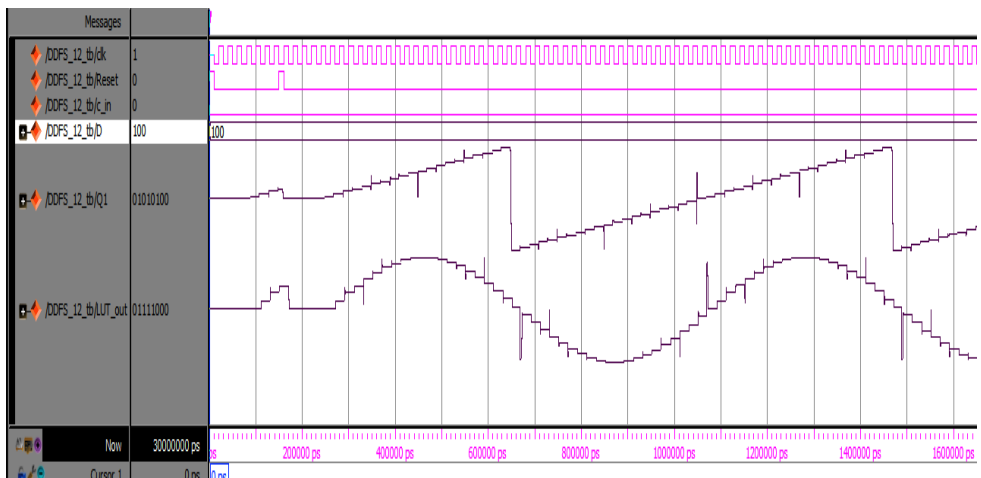
RESULT AND DISCUSSION

For the gate level simulation, the applied timing constraint, the total of the longest clock delay, data delay, and time setup (Tsu) must be less than the chosen clock time within a positive value of the slack. The result of the gate level simulation for the PA and Lookup Table (LUT) output is shown in figure 5. The figure shows that the PA output rapidly accumulates until reaching the (2n-1) point, and then return to (0) and the LUT converts the PA output phase data into amplitude sinusoidal output.

The proposed phase accumulator architecture with CLA adder has been compared with conventional PA that using RCA adder. Table 1 shows the comparison results. The result shows that the Maximum operation frequency (fmax) of the proposed architecture of 12-bit PA is 10.5% higher than PA with RCA adder. The improvement can also be seen for 18-bit PA with 13% advantage.

Table-1. Comparison results of maximum operating frequency (fmax), propagation delay (Tp) and number of registers logic cells

PA Name & No.of Bits	No. Of Bit-Stages	Max. Freq operation (MHz)	Propagation Delay (η Sec)	Registers No.
CLA-12	(4-3)	481.23	2.07	42
RCA-12	(4-3)	431.41	2.3	42
CLA-18	(6-3)	376.93	2.65	62
RCA-18	(6-3)	327.98	3.04	62

CONCLUSION

The proposed 12-bit pipelined phase accumulator PA with CLA adder has been successfully designed and simulated. A comparison has been made with conventional phase accumulator that uses RCA adder. The result showed that the PA with CLA adder runs faster than PA with RCA adder in approximately 10.5% and 13% for 12-bit and 18-bit respectively.

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