



POWER LOSS ANALYSIS MODEL OF A DC-DC BUCK-BOOST CONVERTER WITH AN INTERFACED THREE PHASE INVERTER FOR MEDIUM VOLTAGE APPLICATION



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ABSTRACT

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Keywords

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This paper presents a comprehensive mathematical modelling of a DC to DC Buck-Boost converter. The different power losses associated with the Buck-Boost circuit are also presented. Analysis of the converter power loss is graphically represented at varied duty cycles and load resistance values. A low frequency pulse width modulated inverter is interfaced with the Buck-Boost converter using MATLAB/SIMULINK. For an efficient performance and attenuation of low order harmonics, the low frequency pulse width modulated inverter is substituted with a high frequency pulse width modulated voltage source inverter. A comparison is therefore drawn to show the significant change in the percentage harmonic reduction of the two different frequency modulations. All simulation results are achieved using MATLAB 7.14 version. The simulation results however show that Mosfet switching loss decreases with an increase in the duty cycle whereas Diode and Inductor conduction losses increase with an increase in the duty cycle values.

Contribution/ Originality: This study contributes in the existing literature by showing that at a reduced duty cycle and varied resistance values of a dc-dc buck boost converter, the Mosfet switching loss is increased whereas the Diode and Inductor conduction losses decrease correspondingly with the decrease in the duty cycle.

1. INTRODUCTION

DC to DC converters are extensively applied in power conversion processes for a renewable energy system such as the wind and solar energy applications, distributed generation systems (micro-grids) and dc motor drives [1]. Other applications include d.c power supply for office and telecommunication equipment as well as traction processes. Several measures have been adopted in developing new generations of ac-dc converters that can meet an improved power quality regulation at the same time offer better flexibilities that are required in renewable energy conversion systems [2-5]. Generally, a dc-dc converter can exist in different states which include the buck state, the boost state and the buck-boost state [6]. The multiplicities of some ac-dc converters are formed from the combination of one or two states of the dc-dc converter. A single-switch single stage buck converter was discussed in Juan [7]. This converter is attractive and has a simple controller that produces a high quality input current. The major drawback is that it operates at a high switching frequency of 25 KHz which exposes the switching devices to high voltage stress [8]. The three phase conventional ac-dc boost converter presented in Abdelsalam, et al. [9];

Wijeratne and Moschopoulos [10] has wide electrical applications. Its disadvantage is shown in the use of a boost converter after the diode stage which requires a high switching frequency and also the need for an intermittent pre-charging of the dc capacitor. This topology also has a poor short-circuit protection which can be corrected by incorporating an external dc chopper to the dc-terminals [11]. This paper therefore developed an analytical model for power losses that are inherent in buck-boost converter and ways of adjusting the converter parameters to minimize the magnitude of these losses. The converters parameter adjustments also maximize the performance efficiency of the buck-boost converter. A low frequency pulse-width modulated (LFPWM) inverter is interfaced with the buck-boost converter and this is been compared with a high frequency pulse-width modulated (HFPWM) inverter for harmonic reduction purposes.

2. BASIC BUCK-BOOST CONVERTER OPERATION

A buck-boost converter is frequently applied in the dc to dc power supply stage of most electrical design applications since the output voltage can be regulated to a higher or a lower value than the input voltage. The converter input is normally an unregulated dc voltage or current sources which can be derived from a d.c battery, a rectified a.c source, a photovoltaic panel, a hydrogen based fuel source and electromechanical dc generator [12]. The basic hard-switched buck-boost dc to dc converter has one main unidirectional active semiconductor switch, one major diode and one inductance which functions as a filter and as a current limiting passive element. The input and output capacitors (C_i and C_o) primarily filter the d.c ripples on the input and output terminals. The basic buck-boost converter circuit is presented in Figure 1 and 2. The principle of operation under continuous current mode is usually considered within the intervals of switch (S_m) conduction sequence. During on-state conduction, the input voltage source is directly connected to the inductor (L_m). This results in the accumulation of inductor energy from the source and subsequent supply of energy to the load terminal through the capacitor (C_o). Similarly, in the off-state conduction, the accumulated inductor energy is transferred from the inductor L_m to the capacitor C_o and load resistance R.

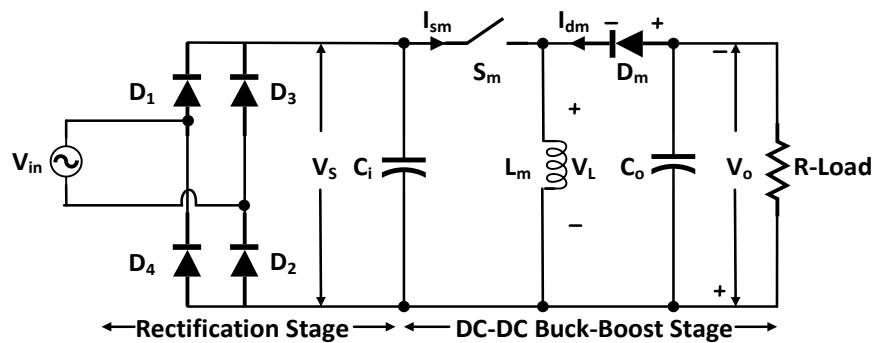


Figure-1. Basic buck-boost converter circuit with rectifiers [5].

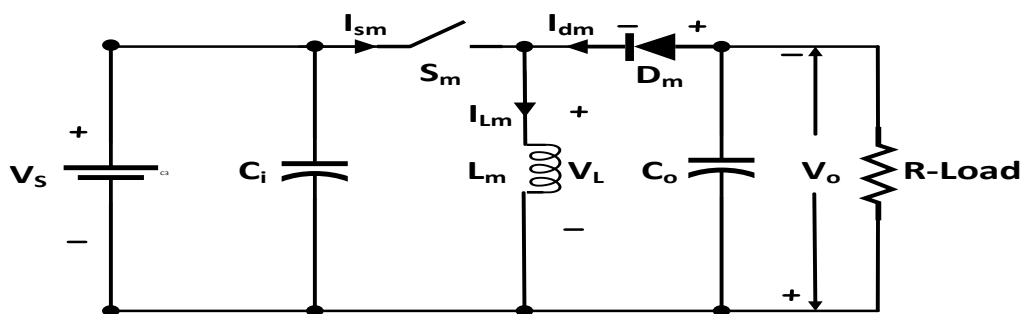


Figure-2. Basic buck-boost converter with a D.C voltage input [6].

- I. At an interval of $0 \leq t \leq DT$ within a cycle, switch S_m is turned on and conducts within this interval while diode D_m which is reverse biased by $V_s - V_o$ does not conduct thus forming an open circuit. The supply current I_m in Figure 2 flows through the path $V_s \rightarrow S_m \rightarrow L_m \rightarrow V_s$ with the input voltage (V_s) directly connected to the inductor L_m . At this stage the output capacitor C_o supplies the needed energy to the output Load.
- II. At an interval of $DT \leq t \leq T$ switch S_m is turned off while diode D_m becomes forward biased by the inductor current I_m and conducts. The inductor current I_m flows through the path $L_m \rightarrow V_o \rightarrow D_m \rightarrow L_m$. At this period energy stored in the inductor is transferred from inductor L_m to output capacitor C_o and output load R .

2.1. Mathematical Model of a Buck-Boost Circuit

At an interval of $0 \leq t \leq DT$ within a cycle, the source voltage V_s is impressed on the inductor. The voltage equation is given by 1.

$$V_L = V_s = L_m \frac{di_L}{dt} \quad (1)$$

By rearrangement and integration of 1 the inductor current is obtained and represented in 2.

$$i_L = \frac{V_s}{L_m} t + I_{L1} \quad (2)$$

At $t = DT$ the inductor current i_L rises to I_{L2} as given by Equation 3.

$$I_{L2} = \frac{V_s}{L_m} DT + I_{L1} \quad (3)$$

The change in the inductor current is represented by Equation 4.

$$\Delta i_L = I_{L2} - I_{L1} = \frac{V_s}{L_m} DT \quad (4)$$

The rate of change in the inductor current is linearly a constant expression as presented in Equation 4.

At $DT \leq t \leq T$ the inductor stored energy is transferred to the load with the voltage equation given by 5.

$$V_L = V_o = L_m \frac{di_L}{dt} \quad (5)$$

By rearrangement and integration of 5 the inductor current is obtained and represented in 6.

$$i_L = \frac{V_o}{L_m} (t - DT) + I_{L2} \quad (6)$$

At $t = T$ the inductor current i_L drops to I_{L1} as given by Equation 7.

$$I_{L1} = \frac{V_o}{L_m} (1 - D)T + I_{L2} \quad (7)$$

The change in the inductor current is represented by Equation 8.

$$\Delta i_L = I_{L2} - I_{L1} = \frac{-V_o}{L_m} (1 - D)T \quad (8)$$

At steady state operation, the net change in inductor current 4-8 is always equal to zero.

$$\frac{V_s DT}{L_m} + \frac{V_o(1 - D)T}{L_m} = 0 \quad (9)$$

$$V_o = -V_s \frac{D}{1 - D} \quad (10)$$

Assuming a lossless state of the converter operation, input power is always equal to the output power.

$$I_s V_s = I_o V_o \text{ and } \frac{V_s}{V_o} = \frac{I_o}{I_s} = \frac{1 - D}{D} \quad (11)$$

$$I_o = I_s \frac{1 - D}{D} \quad (12)$$

Average source current and average inductor current are related by Equation 13.

$$I_s = I_L D \quad (13)$$

Similarly, the output voltage and average inductor current are related by Equation 14.

$$\frac{V_o^2}{R} = V_s I_L D \quad (14)$$

$$I_L = \frac{V_o^2}{V_s \times R \times D} = \frac{V_s D}{R(1 - D)^2} \quad (15)$$

The maximum and minimum inductor currents are obtained from Equation 16 and 17.

$$I_{\max} = I_L + \frac{\Delta I_L}{2} = \frac{V_s D}{R(1 - D)^2} + \frac{V_s DT}{2L_m} \quad (16)$$

$$I_{\min} = I_L - \frac{\Delta I_L}{2} = \frac{V_s D}{R(1 - D)^2} - \frac{V_s DT}{2L_m} \quad (17)$$

The boundary between continuous current mode (CCM) and discontinuous current mode (DCM) is obtained by setting I_{\min} in Equation 17 = 0.

$$\frac{V_s D}{R(1 - D)^2} - \frac{V_s DT}{2L_{\min}} = 0 \quad (18)$$

$$L_{\min} = \frac{(1 - D)^2 R}{2F} \quad (19)$$

Where L_{\min} is the inductor value that determines the boundary between the continuous current mode (CCM) and discontinuous current mode (DCM). The output voltage ripple $\frac{\Delta V_o}{V_o}$ for the buck-boost converter is derived from 20, 21 and 22.

$$\Delta Q = \frac{V_o}{R} DT = C\Delta V_o \quad (20)$$

$$\Delta V_o = \frac{V_o DT}{RC} = \frac{V_o D}{RCF} \quad (21)$$

$$r = \frac{\Delta V_o}{V_o} = \frac{D}{RCF} \quad (22)$$

The power losses and the efficiency of the Buck-Boost Converter are achieved with the aid of the equivalent circuit diagram presented in Figure 3.

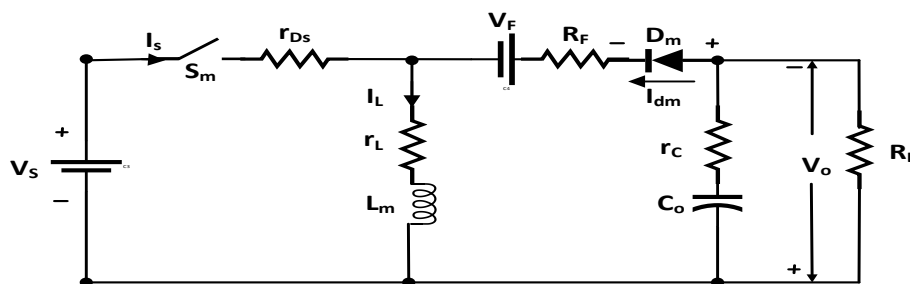


Figure-3. Buck-boost equivalent circuit with parasitic resistance and diode forward voltage [11].

The following power losses associated with the Buck-boost equivalent circuit were considered:

- I. The MOSFET conduction loss from the r_{DS} (On-resistance or drain-source resistance).
- II. The high frequency switching loss.
- III. The diode forward resistance (R_F) loss.
- IV. The diode forward voltage loss.
- V. The inductor conduction loss from (r_L).
- VI. The power loss from the filter capacitor resistance.

The MOSFET r_{DS} conduction loss is given by 23.

$$P_{r_{DS}} = r_{DS} I_{srms}^2 = \frac{Dr_{DS}I_o^2}{(1 - D)^2} = \frac{Dr_{DS}P_o}{(1 - D)^2 R_L} \quad (23)$$

The high frequency switching loss is given by 24.

$$P_{sw} = F_S C_o (V_1 + V_o)^2 = \frac{F_S C_o R_L P_o}{D^2} \quad (24)$$

Total power dissipation in the MOSFET (excluding the drive power) is expressed in Equation 25.

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \left[\frac{Dr_{DS}}{(1-D)^2 R_L} + \frac{F_S C_0 R_L}{2D^2} \right] P_0 \quad (25)$$

The power loss in the diode forward resistance is presented in Equation 26.

$$P_{RF} = R_F I_{Drms}^2 = \frac{R_F I_0^2}{1-D} = \frac{R_F P_0}{(1-D)R_L} \quad (26)$$

The power loss associated with the diode forward voltage is given by Equation 27.

$$P_{VF} = V_F I_D = V_F I_0 = \frac{V_F P_0}{V_0} \quad (27)$$

The overall diode conduction loss is given by Equation 28.

$$P_D = P_{VF} + P_{RF} = V_F I_0 + \frac{R_F I_0^2}{1-D} = \left[\frac{V_F}{V_0} + \frac{R_F}{(1-D)R_L} \right] P_0 \quad (28)$$

The inductor conduction loss is represented in Equation 29.

$$P_{rL} = \frac{r_L I_0^2}{(1-D)^2} = \frac{r_L P_0}{(1-D)^2 R_L} \quad (29)$$

The power loss in capacitor filter is presented in 30.

$$P_{rc} = r_c i_{crms}^2 = \frac{Dr_c I_0^2}{1-D} = \frac{Dr_c P_0}{(1-D)R_L} \quad (30)$$

The overall power loss is represented in 31-33.

$$P_{LS} = P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rc} \quad (31)$$

$$P_{LS} = \frac{Dr_{DS} I_0^2}{(1-D)^2} + F_S C_0 (V_1 + V_0)^2 + V_F I_0 + \frac{R_F I_0^2}{1-D} + \frac{r_L I_0^2}{(1-D)^2} + \frac{Dr_c I_0^2}{1-D} \quad (32)$$

$$P_{LS} = \left[\frac{Dr_{DS} + r_L}{(1-D)^2 R_L} + \frac{F_S C_0 R_L (1 + M_{VDC})^2}{M_{VDC}^2} + \frac{V_F}{V_0} + \frac{R_F + Dr_c}{(1-D)R_L} \right] P_0 \quad (33)$$

$M_{VDC} = \frac{V_0}{V_1}$ = dc voltage transfer function.

The converter efficiency is given by Equations 34.

$$\eta = \frac{P_0}{P_0 + P_{LS}} = \frac{1}{1 + \frac{P_{LS}}{P_0}} \quad (34)$$

The d.c current transfer function of the buck-boost converter is represented by Equation 35.

$$M_{VDC} = \frac{I_0}{I_1} = \frac{1-D}{D} \quad (35)$$

The converter efficiency in terms of voltage and current transfer function is given by Equation 36.

$$\lambda = \frac{P_o}{P_i} = \frac{V_o I_o}{V_i I_i} = M_{VDC} \times M_{IDC} = \frac{(1-D)M_{VDC}}{D} \quad (36)$$

The voltage transfer function of a lossy buck-boost is represented in Equation 37.

$$M_{VDC} = \frac{\lambda}{M_{IDC}} = \frac{(1-D)}{D} \quad (37)$$

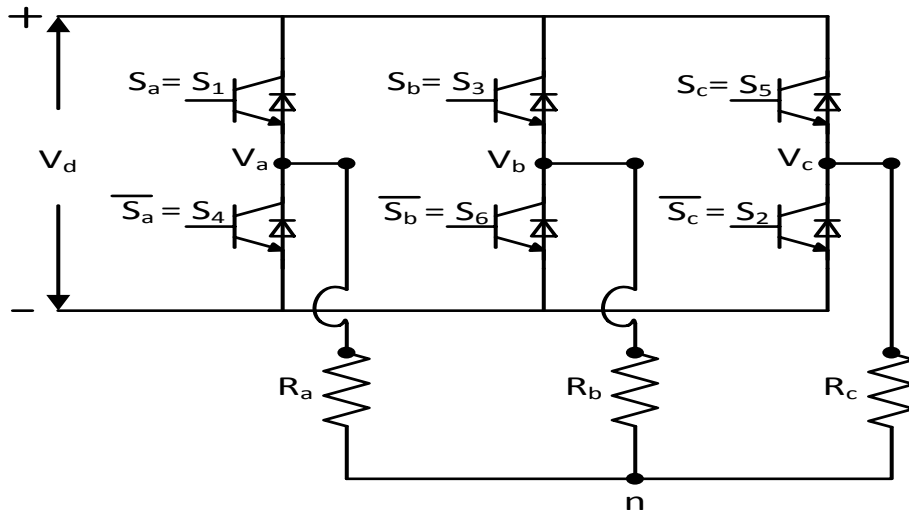


Figure-4. Three phase voltage source inverter circuit diagram [12].

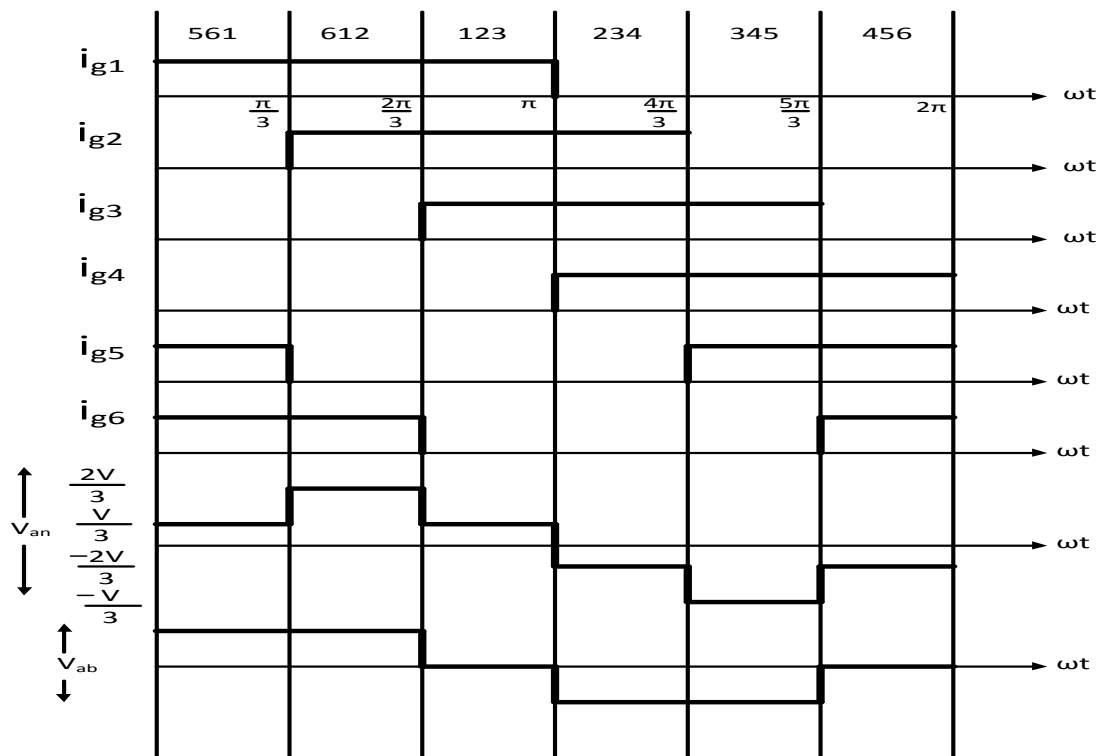


Figure-5. Per cycle variation of low frequency switching/gating signals of three phase inverter [12].

3. THREE PHASE VOLTAGE SOURCE INVERTER MODEL

A voltage source inverter is an electrical device that converts a direct current (d.c) voltage to its equivalent alternating current (a.c) voltage [13-15]. The a.c voltage and frequency may be varying or constant in nature

depending on the application. A voltage fed inverter always has a stiff dc voltage source at the input terminal. This implies that its Thevenin impedance at every time interval is ideally zero. The d.c voltage is usually obtained from a battery source, fuel cell or photovoltaic cell [16-18]. Voltage-fed inverters are used extensively in major electrical applications such as uninterruptible power supplies (UPS), induction heating, active harmonic filters, static var compensators and flexible alternating current transmission systems devices (FACTS-DEVICES) [19-23]. The three phase voltage source inverter circuit diagram is presented in Figure 4. The inverter switching control systems are considered in terms of low frequency and high frequency carrier modulation. The low frequency pulse width modulation pattern per cycle angular spacing is shown in Figure 5.

The high frequency switching signals is accomplished by comparing a phase disposition carrier signals with a modulating or a reference signal. The high frequency carrier signal is generated with the aid of the Simulink ramp block diagram in accordance with Equation 38.

$$tr_1 = \begin{bmatrix} 0 & \frac{1}{2f_c} & \frac{1}{f_c} \\ x-1 & x & x-1 \end{bmatrix} \quad (38)$$

tr_1 represents the triangular or carrier waves for the inverter switching signal, x represents the amplitude of the respective triangular or carrier waveforms and f_c represents the switching frequency of the inverter power switches. The modulating signal of the voltage source inverter is represented in Equation 39.

$$V = A_m \sin \theta \quad (39)$$

The basic algorithm for the switching signal is achieved with Equation 40.

$$\begin{cases} \text{If } V > tr_1; S_a = 1; \bar{S}_a = 0; \\ \text{else } V < tr_1; S_a = 0; \bar{S}_a = 1 \end{cases} \quad (40)$$

The overall circuit diagram for the DC-DC Buck-Boost converter with an interfaced Inverter circuit diagram is shown in Figure 6.

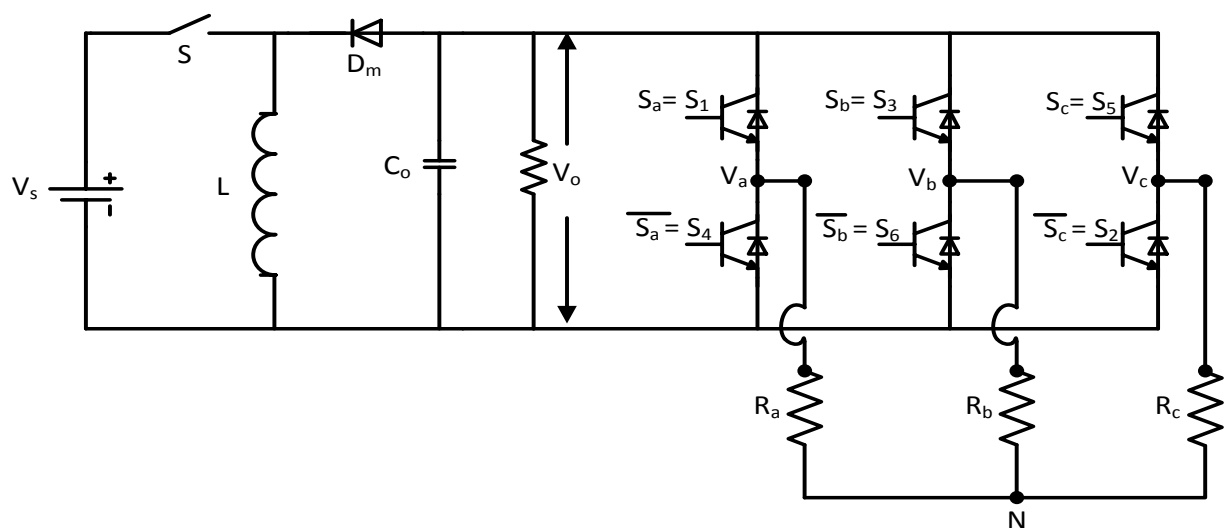


Figure-6. A DC-DC buck-boost with an interfaced inverter circuit diagram [13].

4. SIMULATION RESULTS AND DISCUSSION

The simulation results for the DC-DC Buck-Boost converter were realized with the parameter shown in Table 1 and 2. The simulation was done at a duty cycle values of 0.25, 0.5 and 0.75 respectively. In Figure 7 it is observed that at an input voltage of 100V, the converter produced a voltage of -33.33V at a duty cycle of $D = 0.25$. This

entails a Bucking operation which is in conformity with Equation 10 since $V_s < V_o$ when $D < 0.5$. In Figure 8 at a duty cycle value of $D = 0.5$, the input voltage $V_s = 100V$. This obviously corresponds to the magnitude of the output voltage $V_o = |-100V|$. This value clearly agrees with Equation 10. The converter at this condition operates in its normal state with input voltage equal to the output voltage. Similarly, for a slight increase in the duty cycle value from 0.5 to 0.75, the output voltage increases geometrically in magnitude to a peak value of $V_o = |-300V|$ as shown in Figure 9. This operation at $D > 0.5$ or $D = 0.75$ indicates a Boosting operation of the converter. In Figure 10-13 the plots of various Losses associated with the Buck-Boost converter with respect to varied load resistance and duty cycle were presented. It is evidently shown in Figure 11-13 that when the duty cycle D is close to zero value, the conduction losses which include the diode conduction loss, inductor conduction loss and capacitive discharge are low in value. Conversely, the MOSFET switching loss peaks at a high value at low duty cycle since the input voltage is high at a fixed value of the output voltage. The conduction losses therefore increase rapidly as the duty cycle value is increased to 0.5 and above with a corresponding decrease in the MOSFET switching loss. The efficiency in line with the increase in the duty cycle from 0-0.5 increases and peaks at $D = 0.5$ as shown in Figure 14. At a value of $D > 0.5$, the efficiency decreases to zero when $D = 1$. In Figure 15 and 16 the waveforms for the Phase A output voltage and total harmonic distortion for the Low Frequency and High Frequency Pulse Width modulated inverter were presented. It is obviously shown from the spectral analysis that the fundamental value of the output voltage amplitude is 127.5V for the Low frequency PWM which is far less than the 154.5V obtained for the high frequency PWM. The %THD value of 30.94% contains more harmonics for the low frequency pulse width modulated inverter when compared with the 28.68% obtained for the high frequency pulse width modulated inverter. This implies that at a high switching frequency, low order harmonics below the carrier frequency are eliminated for a medium and high voltage application.

Table-1. DC-DC buck-boost simulation parameters [15].

Simulation parameters	Values
Input voltage	100V
Switching frequency	10KHZ
Inductance value	25Mh
Capacitance value	2200 μ F
Load resistance value	15 Ω
Duty cycles	0.25, 0.50 and 0.75

Table-2. DC-DC buck-boost equivalent circuit parameters [15].

Simulation parameters	Values
Internal resistance of the MOSFET r_{DS}	0.11 Ω
Diode forward voltage V_F	0.7V
Diode forward resistance	20m Ω
Capacitance value	2200 μ F
Load resistance values	5 Ω to 50 Ω
Duty cycles	0 to 1.0

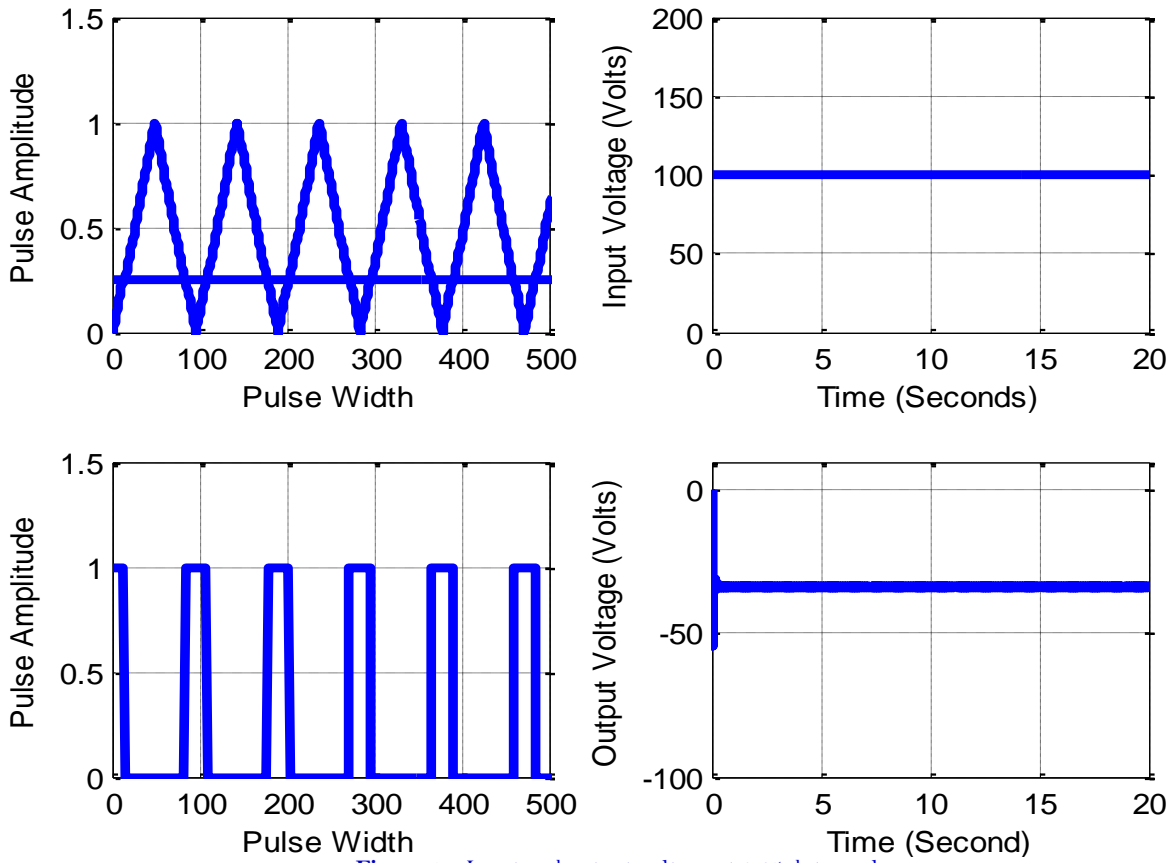


Figure-7. Input and output voltage at 0.25 duty cycle.

Source: Simulation result.

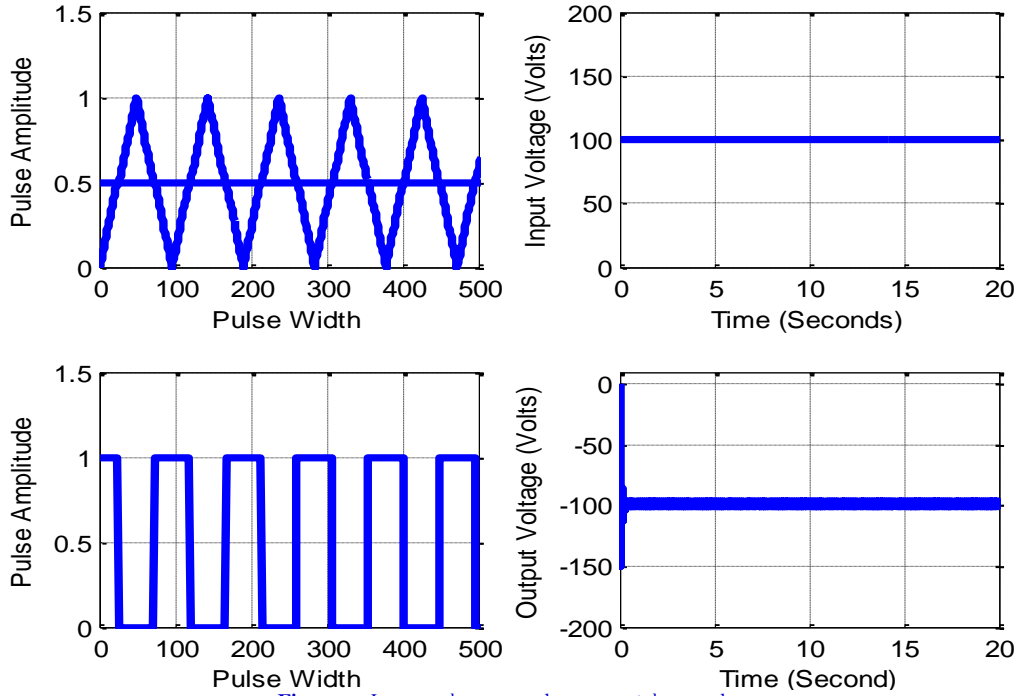


Figure-8. Input and output voltage at 0.5 duty cycle.

Source: Simulation result.

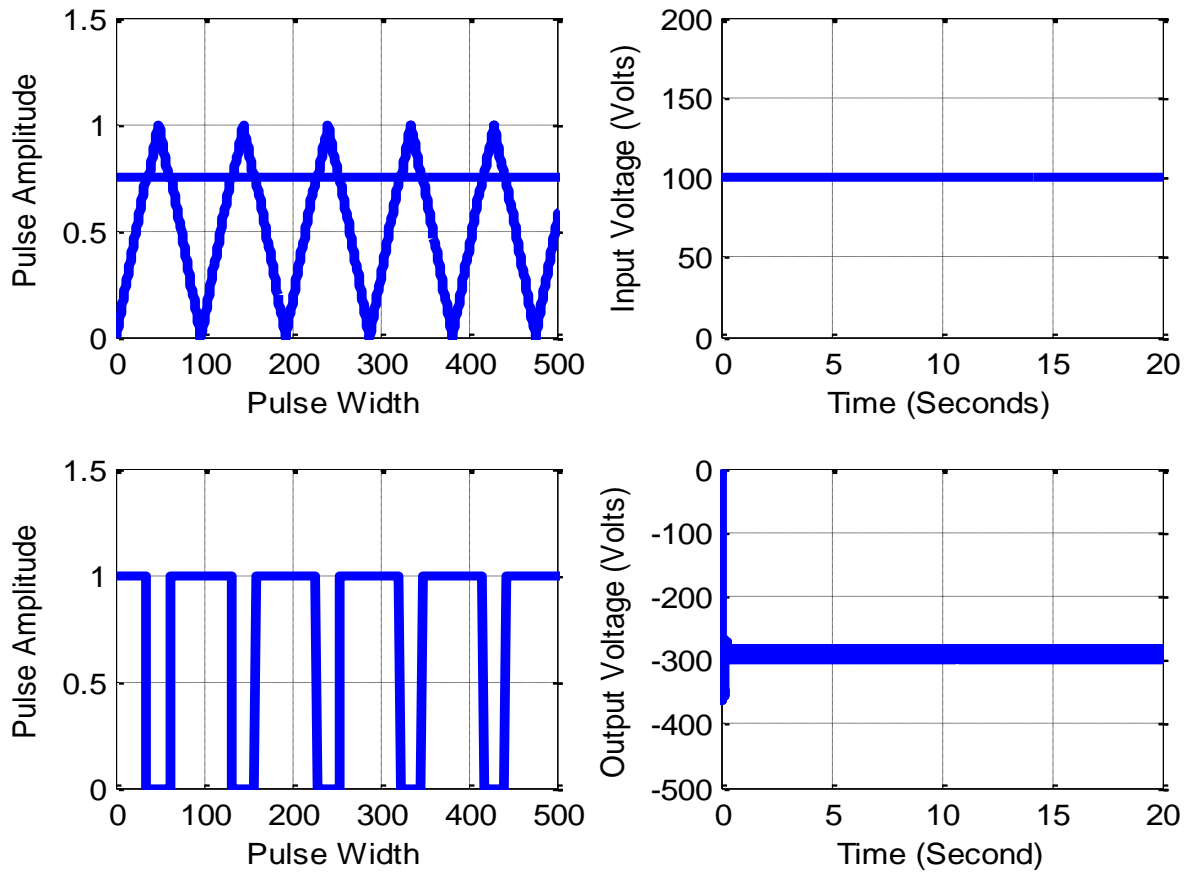


Figure-9. Input and output voltage at 0.75 duty cycle.

Source: Simulation result.

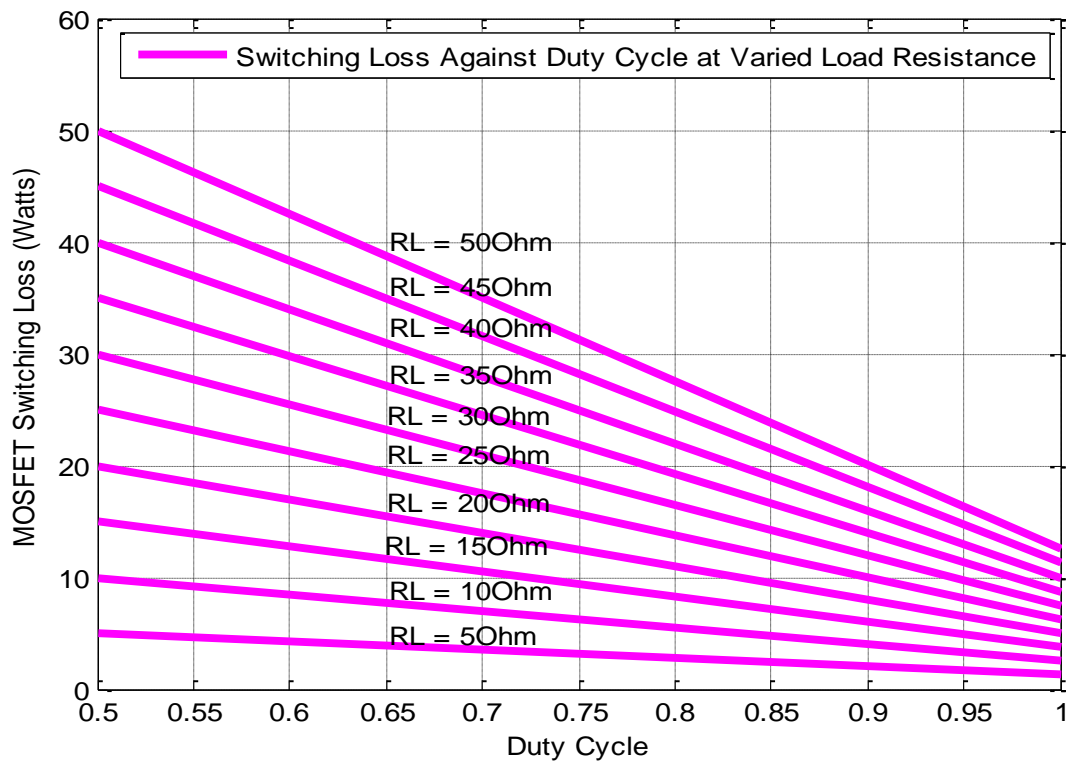


Figure-10. MOSFET switching loss against duty cycle.

Source: Simulation result.

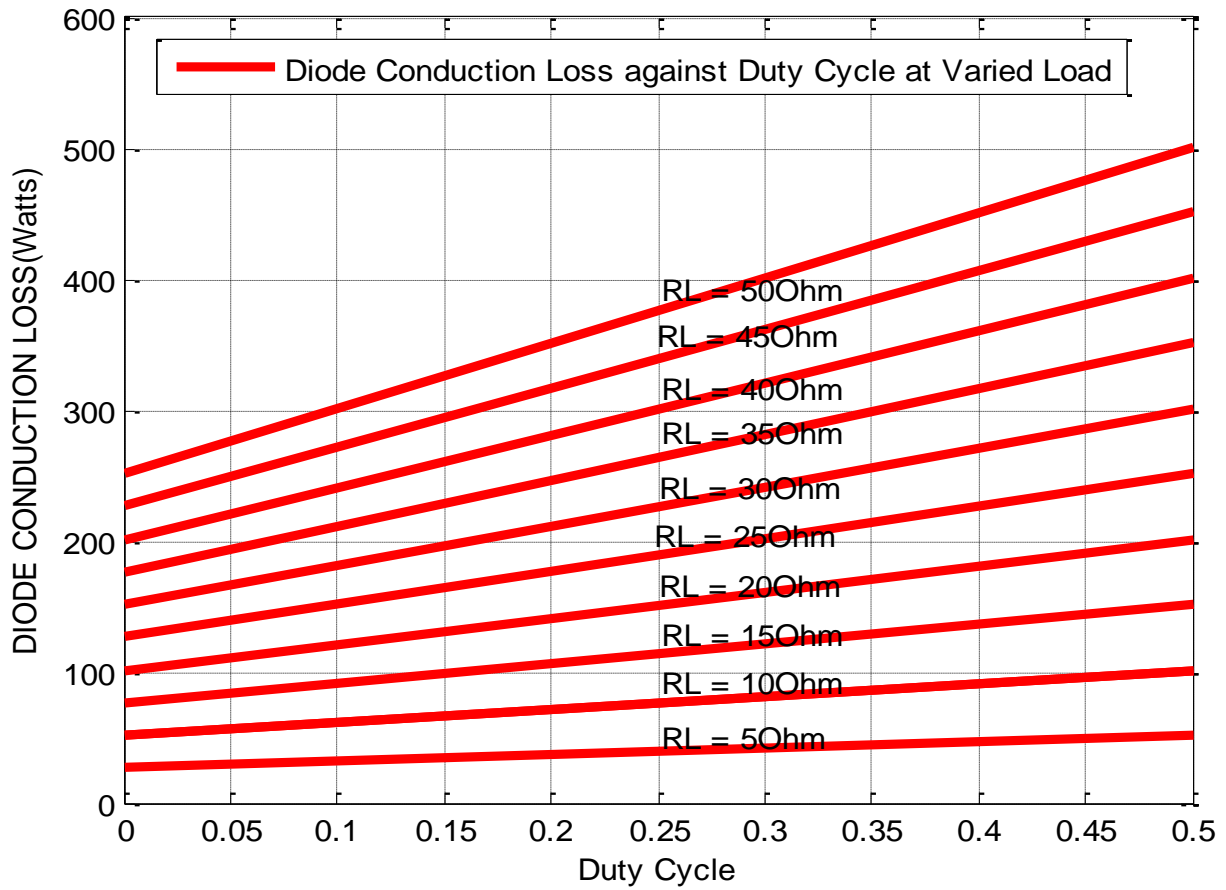


Figure-11. Diode conduction loss against duty cycle.

Source: Simulation result.

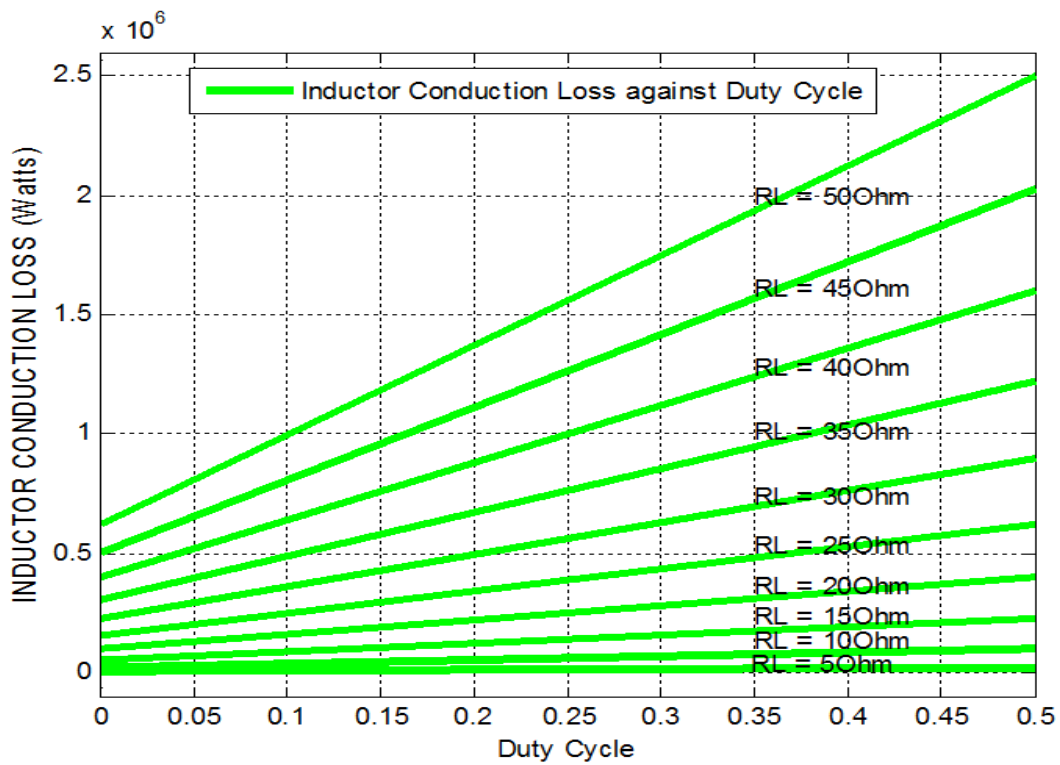


Figure-12. Inductor losses against duty cycle.

Source: Simulation result.

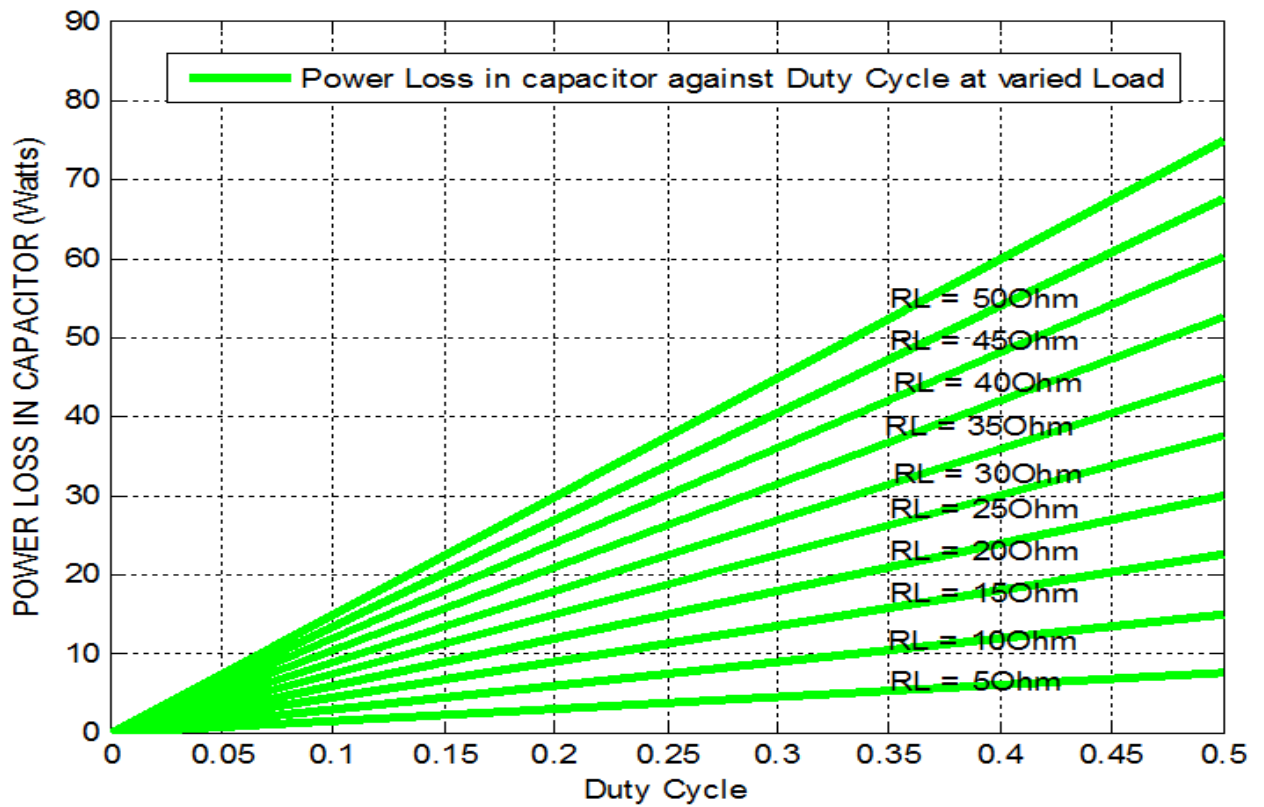


Figure-13. Power loss in capacitor against duty cycle.

Source: Simulation result.

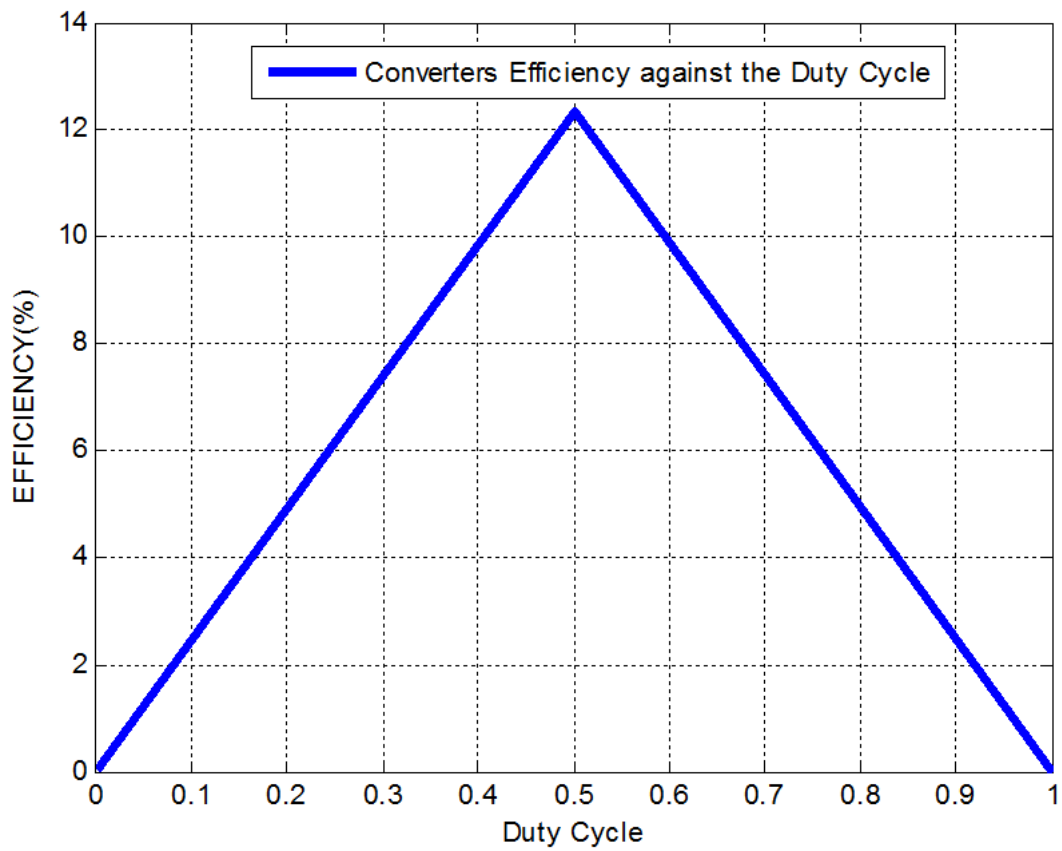


Figure-14. Converters efficiency against duty cycle.

Source: Simulation result.

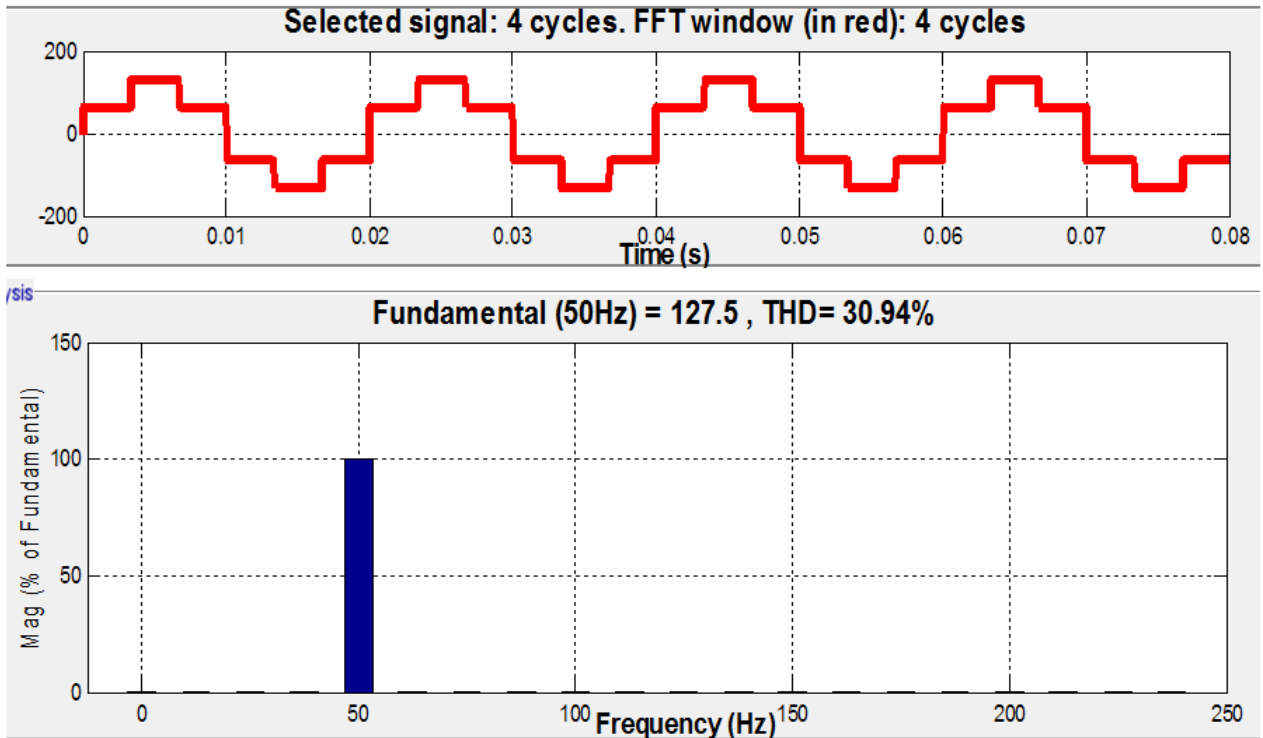


Figure-15. Phase A voltage and THD for LFPWM.

Source: Simulation result.

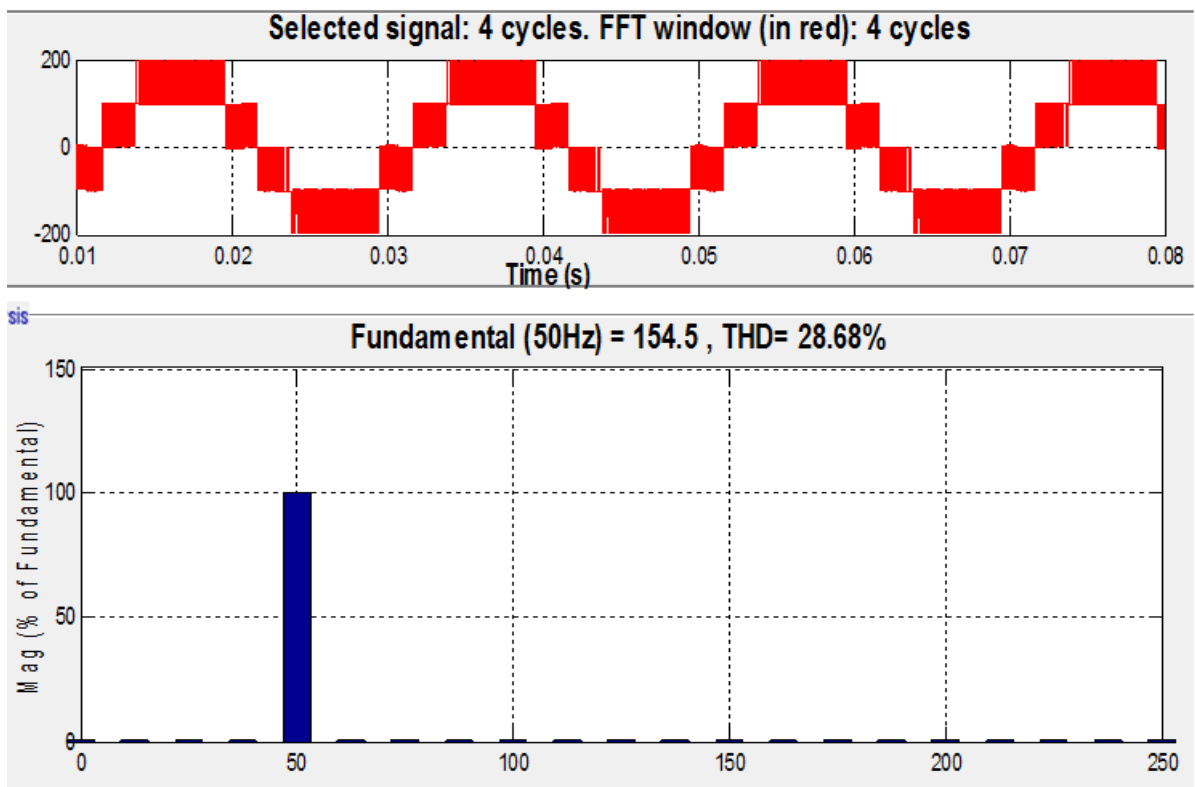


Figure-16. Phase A voltage and THD for HFPWM.

Source: Simulation result.

5. CONCLUSION

In this work, a thorough analysis of the mathematical modelling of a Buck-Boost dc-dc converter was made with respect to the converter losses at varied duty cycle and load resistance value. The simulation results achieved with MATLAB 7.14 showed that when the duty cycle D is close to zero, the conduction losses are low but the

switching loss is usually high. Hence, the efficiency decreases to zero at a unity duty cycle as indicated in the simulation waveforms. The values obtained from the simulation waveforms for the Bucking State and Boosting state clearly showed a conformity in values when the converter parameters are substituted in the modeled equation for the Buck-Boost converter. Similarly, at a high frequency pulse width modulated inverter, low order harmonics below the carrier frequency are always eliminated for a medium and high voltage application.

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