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Piezoelectric energy harvesting interface with fast open-circuit voltage sampling

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ABSTRACT

This paper presents a piezoelectric energy harvesting interface with fast open-circuit voltage (V_{OC}) sampling and a wide operating frequency range. The fractional open-circuit voltage (FOCV) method is the primary method for maximum power point tracking (MPPT) in energy harvesting systems, due to its easy implementation and relatively low cost. For this method to be efficient, it is necessary to shorten the time required for V_{OC} sampling. To minimize power loss due to V_{OC} sampling, a novel technique is proposed that is capable of sampling the V_{OC} within a time shorter than half a cycle by using an adaptive tracking pulse instead of conventional fixed ones. We also present a peak detector design technique that can operate across a broad frequency spectrum and adapt to diverse vibration scenarios. The proposed technique reduces the duty cycle of the tracking pulse to 0.42%, which is 3.7 times smaller than the conventional 1.56%. The proposed circuit, designed using a 0.35µm complementary metal oxide semiconductor (CMOS) process, consumes just 94nA at 100Hz, 3V $V_{OC,}$ and a 1kΩ load. In a 2~4V V_{OC} range and a 15~500Hz frequency range, the MPPT efficiency exceeds 95%, peaking at 99.9%, and the power efficiency remains over 93%, reaching a maximum of 97.7%.

Contribution/ Originality: Compared to the existing FOCV-based MPPT techniques applied to piezoelectric energy harvesting systems, the proposed technique in this study has the advantage of minimizing the power loss rate because the open-circuit voltage sampling time is the shortest using an adaptive tracking pulse.

1. INTRODUCTION

Various fields have widely used energy harvesting technology as a substitute or auxiliary means for batteries in recent times. In particular, in the case of wireless sensor networks, where battery replacement is practically impossible, harvesting ambient energy and supplying power to sensor nodes is becoming an essential method [1]. Energy transducers output the maximum available power at their respective maximum power point (MPP). Since the MPP varies with the surrounding environment, maximum power point tracking (MPPT) control is necessary. Especially in systems with very small sizes, such as miniature-size sensor nodes, the form factor of energy transducers is also small, resulting in a very limited amount of harvestable energy. In such cases, the importance of MPPT becomes even more pronounced.

Among various energy sources, piezoelectric energy harvesters (PEHs), primarily utilized in systems that scavenge vibrational energy [2-17] generate alternating current (AC)-type signals, thus requiring rectifiers (RECs) at the output to convert them into direct current(DC) signals. Various types of PEH rectifiers, such as a full-bridge rectifier (FBR) [2-4] a synchronous electric charge extraction (SECE) rectifier [5] a synchronized-switch harvesting-on-inductor (SSHI) rectifier [6-8] and a synchronized-switch harvesting-on-capacitor (SSHC) rectifier [9] have been developed and used in vibration energy harvesting systems. The parallel-SSHI rectifiers, which have received increasing attention recently, exhibit excellent energy extraction capabilities from PEHs. However, various factors influence their MPP, making the practical application of MPP, making the practical application of MPPT challenging [7]. Furthermore, since the open-circuit voltage (V_{OC}) of the SSHI circuit is usually very high, the time to reach V_{OC} is very long. Due to voltage limits in the process being used, it is no longer possible to use the fractional open-circuit voltage (FOCV) method in real life [10]. In Li, et al. [7] an MPPT circuit based on a hill-climbing method has been implemented instead of the FOCV method, but this necessitates complex power monitoring circuits, resulting in a relatively high current consumption of 1.57 µA.

The FOCV method periodically opens the output of the piezoelectric energy generator (PEG), which consists of a PEH and a REC, and samples the V_{OC} to determine the MPP voltage (V_{MPP}). For the FOCV method to be efficient, it is crucial to minimize the duration when the PEG output is open, referred to as the MPP tracking phase (MTP), while maximizing the energy harvesting phase (EHP). In Chew and Zhu [4] a technique has been proposed that employs a high-pass filter and a differentiator to directly sense V_{MPP} without the need to open the output of the PEG. While this method maximizes the EHP to 100%, it is restricted to low frequencies (2~10Hz) and suffers from a relatively large MPP tracking error of ±30%.

In conventional FOCV methods, large-value capacitors were employed on the REC's output to sample the V_{OC} (1µF [3] and 0.5µF [11]). As a result, it takes a long time to settle on the V_{OC} and the time required for V_{OC}sampling is at least 2 cycles. Researchers have proposed a technique using a small-sized capacitor (several nF to tens of nF) to reduce the time required to reach Voc [2, 10]. By utilizing small-sized capacitors, the output of the FBR reaches V_{OC} in a short time, and the V_{OC} is sensed using a peak detector or a differentiator. Consequently, one-cycle V_{OC} sampling becomes achievable [2].

This paper proposes a novel technique for sampling Voc within a time frame shorter than half a cycle of the PEH excitation. It is possible to minimize the MTP interval and maximize the EHP interval by using an adaptive tracking pulse instead of using fixed 1-cycle or 2-cycle tracking pulses. By employing a small-sized capacitor at the REC output and utilizing a clock synchronized with PEH excitation, the time for PEG output to reach V_{OC} is reduced to approximately a quarter cycle, and the MTP interval can be minimized by switching to the EHP immediately after V_{OC} sampling and V_{MPP} update. The proposed circuit is designed to operate across a wide frequency range (up to 500Hz) and a broad V_{OC} range of 2V to 4V, enabling its application in various environments. Furthermore, the circuit employs various low-voltage low-power techniques, enabling the constituent blocks only during the necessary operational phases to effectively minimize power consumption.

2. PROPOSED MPPT INTERFACE CIRCUIT

2.1. Overall Architecture

The structure of the proposed MPPT interface circuit for piezoelectric energy harvesting is illustrated in Figure 1. Vibrational energy is converted into electrical energy through the PEH. The AC-type signal produced by the PEH is transformed into a DC signal by the REC and then stored in the storage capacitor C_{BF}. The voltage applied to C_{BF}, denoted as V_{BF}, is utilized as the power supply for the interface circuit. When V_{BF} is boosted to a sufficient voltage (approximately 1.3V) capable of driving the MPPT controller circuit, an enable (EN) signal is generated at the voltage detector (VD), initiating the controller's operation.

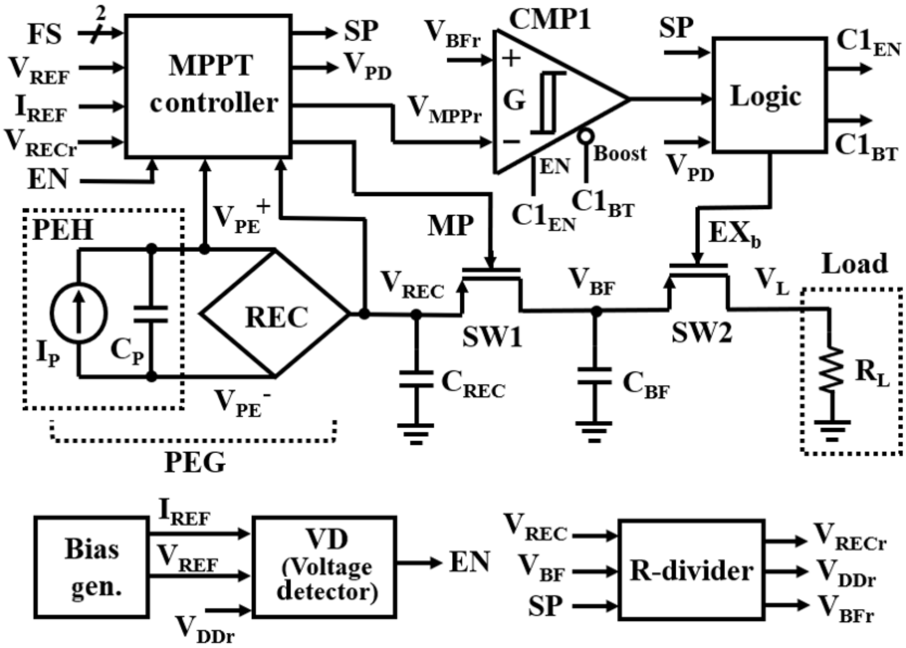
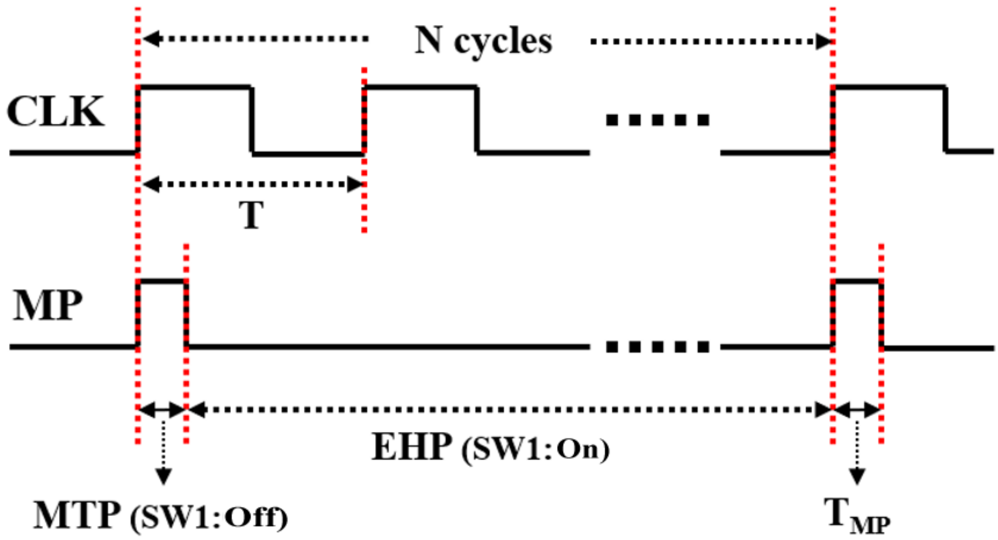


Figure 1. Simplified block diagram of the proposed MPPT interface circuit.



$$f_{MP} = \frac{1}{N} \qquad \delta_{MP} = \frac{T_{MP}}{N \cdot T} \times 100\ (\%)$$

Figure 2. Timing diagram of the MPPT pulse.

The MPPT controller generates an MPPT pulse (MP) to periodically open the output of the PEG, and when the switch SW1 is opened, it samples the output voltage (i.e., V_{OC}) of the PEG to generate the V_{MPP}. The shorter the MTP (when SW1 is off) compared to the EHP (when SW1 is on), the duty cycle (δ_{MP}) of the MP signal decreases, resulting in improved system efficiency. As illustrated in Figure 2, the clock synchronizes with PEH excitation to generate the MP signal once every N cycle. A lower frequency of MP occurrence (lower f_{MP}, i.e., larger N) reduces δ_{MP}, thus minimizing power losses. However, in an environment where MPP changes frequently, if f_{MP} is too small, MPPT cannot be performed in a timely manner, resulting in greater power loss. Therefore, in this paper, a 2-bit frequency selection signal FS is employed to allow the system to adapt to the applied environment, enabling the selection of f_{MP} from among 1/8, 1/16, 1/32, and 1/64.

The comparator CMP1, equipped with a hysteresis function, compares V_{BF} and V_{MPP} to generate the energy extraction signal EX_b, determining the on/off state of SW2. During the EHP, when the voltage corresponding to the output of the PEG, V_{BF}, becomes lower than $V_{MPP,min}$, SW2 opens (ESP: Energy Storage Phase), allowing the harvested energy to be stored in C_{BF}. When V_{BF} exceeds $V_{MPP,max}$, SW2 turns on (EXP: Energy Extraction Phase), supplying the energy stored in C_{BF} to the load. Consequently, the output voltage of the PEG is band-band controlled between $V_{MPP,min}$ and $V_{MPP,max}$ determined by the hysteresis width characteristic of the CMP1.

The operation modes according to the on/off status of switches SW1 and SW2 are summarized in Table 1. When the proposed circuit is directly connected to the load, it can operate in an active/sleep mode, remaining in a sleep mode during the ESP and functioning only during the EXP [1, 11]. Additionally, in cases where continuous operation is required, a DC-DC converter can be connected to the interface circuit output to supply stabilized voltage to the energy buffer and drive the application circuit [3, 11].

Table 1. Operation modes according to switch on/Off status.

SW1	SW2	Operation mode
Off	Off	MTP & ESP
Off	On	MTP & EXP
On	Off	EHP & ESP
On	On	EHP & EXP

2.2. Proposed V_{oc} Sampling Scheme

The clock used within the MPPT controller is generated in synchronization with the V_{PE}^{+} signal, making the clock period T equivalent to the vibration period of the PEH. In the existing methods for sampling V_{OC}, fixed tracking pulses with a duration corresponding to 1 cycle [2] or 2 cycles [3, 11] were utilized. In these methods, a drawback is that even after the peak value is sampled, SW1 remains open for a predetermined pulse duration, preventing energy harvesting during that period.

In this paper, to address this issue, an adaptive tracking pulse MP is employed, as depicted in Figure 3. A counter periodically sets the MP signal to a high state. Once V_{OC} sampling and V_{MPP} update are completed, it immediately transitions to a low state, eliminating unnecessary pulse width periods. When the MP signal goes high, SW1 opens, causing V_{REC} to increase up to V_{OC}. Once the peak of V_{REC} is detected by a peak detector, a short-duration sampling pulse (SP) of approximately 40μs (T_{SP}) is generated. During this interval, V_{OC} sampling and updating of the V_{MPP} corresponding to half of V_{OC} are completed. The falling edge of the MP signal is defined by the falling edge of the SP signal, resulting in a pulse width of T_{MP}, which is smaller than half a cycle ($0.25T+T_{SP}$).

Figure 3 illustrates waveforms when the PEH excitation frequency is 100Hz and the V_{OC} changes from 4V to 3V before and after the generation of the MP signal. While SP is high, the V_{MPPr} corresponding to 1/4 of V_{MPP} is updated from 500mV to 375mV, and V_{REC} changes from 2V to the new MPP value of 1.5V. The pulse width T_{MP} corresponding to MTP is 2.7ms, which is 27% of one cycle (10ms) and is smaller than half a cycle, and actually closer to a quarter-cycle. When the MP occurs once every 64 cycles ($f_{MP}=1/64$), the duty cycle δ_{MP} is reduced by a factor of 1.9x/3.7x/7.4x compared to the fixed pulse widths of 0.5T/1T/2T, which have duty cycles of 0.78%, 1.56%, and 3.13%. This reduction in duty cycle corresponds to a theoretical improvement in power efficiency of 0.36% 1.14%, or 2.71% for each case. Simulation results indicate a 0.69% improvement in power efficiency for the proposed circuit when $f_{MP}=1/32$, compared to the results obtained with a fixed T_{MP} of 0.5T.

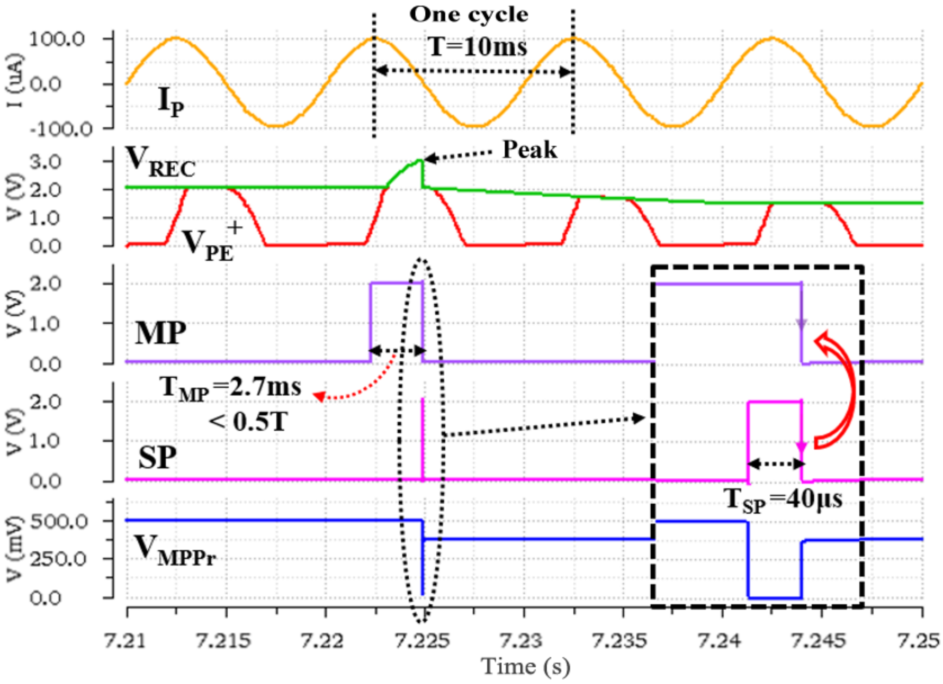


Figure 3. Simulated waveforms for the MPP tracking process.

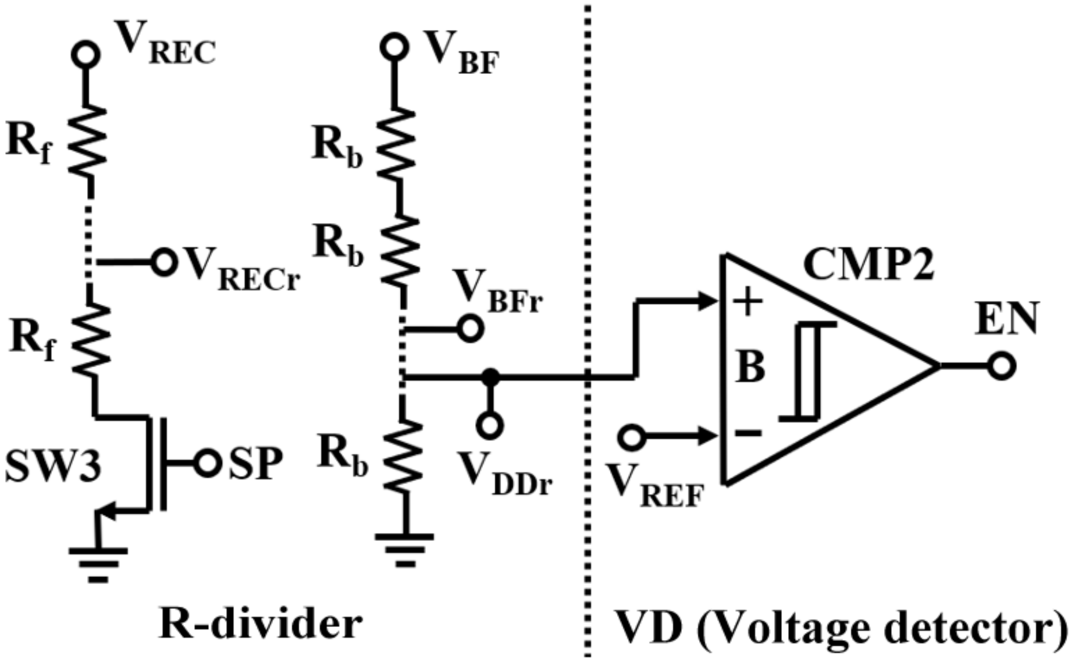


Figure 4. R-divider and voltage detector.

2.3. Piezoelectric Energy Harvester (PEH)

The PEH can be modeled as a parallel circuit of a current source and a capacitor, as shown in Figure 1. The current source can be expressed using the following equation:

$$i_P(t) = I_P \sin(2\pi f t) \quad (1)$$

Here, the amplitude I_P is determined by the material or size of the PEH and the magnitude of vibration, and the frequency f corresponds to the vibration frequency [11]. The value of the internal capacitor C_P typically ranges from tens of nF to hundreds of nF [6, 15] and it exhibits relatively consistent characteristics across a wide range of vibration frequencies. The value of C_P used in this design is 53nF. The theoretical maximum power, V_{OC}, and V_{MPP} that can be obtained from the PEG are given by (2) [12].

$$P_{max} = f C_P V_{OC}^2, \quad V_{OC} = \frac{I_P}{2\pi f C_P}, \quad V_{MPP} = \frac{V_{OC}}{2} (2)$$

In this design, the target range for V_{OC} is 2V to 4V, and thus, the V_{BF} range during MPPT operation becomes 1V to 2V. The minimum power supply voltage (V_{BF}) required for circuit operation limits the minimum value of VOC, while the voltage limitations of the employed fabrication process determine the maximum value.

To accommodate various environments, the targeted vibration frequency range is from a few Hz to 500Hz, aiming for a wide frequency coverage. This frequency range encompasses the frequencies of low-level vibration sources [18] and also mostly includes the resonant frequencies of PZT (lead zirconate titanate) components,as in Sarker, et al. [19]. To verify the performance of the designed circuit at the minimum, intermediate, and maximum V_{OC} values of 2V, 3V, and 4V, the values of I_P used are obtained by multiplying 0.667µA, 1.0µA, and 1.333µA with the vibration frequency f, respectively. Table 2 summarizes the ideal characteristics of the PEH for each case. The maximum achievable output power within the given frequency range is 424.6µW at f=500Hz and I_P=666.5µA.

Table 2. Ideal characteristics of the PEH at test points.

$I_P(\mu A)$	$V_{OC}(V)$	$V_{MPP}(V)$	$P_{max}(\mu W)$ $(f = 15Hz)$	$P_{max}(\mu W)$ $(f = 100Hz)$	$P_{max}(\mu W)$ $(f = 500Hz)$
$0.667 \cdot f$	2.003	1.0015	21.263	21.263	106.31
$1.0 \cdot f$	3.003	1.5015	47.793	47.793	286.76
$1.333 \cdot f$	4.003	2.0015	84.923	84.923	424.61

2.4.Voltage Detector and Comparators

As shown in Figure 4, the voltage detector (VD) compares the divided V_{BF} (V_{DDr}) with the V_{REF} (approximately 0.4V) generated from the bias generator. This comparison triggers the generation of the enable signal (EN) to activate the MPPT controller. The storage capacitor, C_{BF}, has a relatively large value of 47uF, causing changes in V_{BF} to be relatively slow. As a result, relatively large resistors (1MΩR_b in a quantity of 60) are used in the R-divider connected to the V_{BF}-ground path to minimize current consumption. For the V_{REC}-ground path used to generate V_{RECr} in the V_{OC} sampling circuit, relatively small resistors (100kΩ R_f in a quantity of 4) are employed to consider the required speed for updating V_{MPP}. In this path, while the overall resistance values are relatively small, the average current consumption is very low because the SW3 is only turned on during the interval when the SP, which is used for updating V_{MPP}, is high (approximately 40µs).

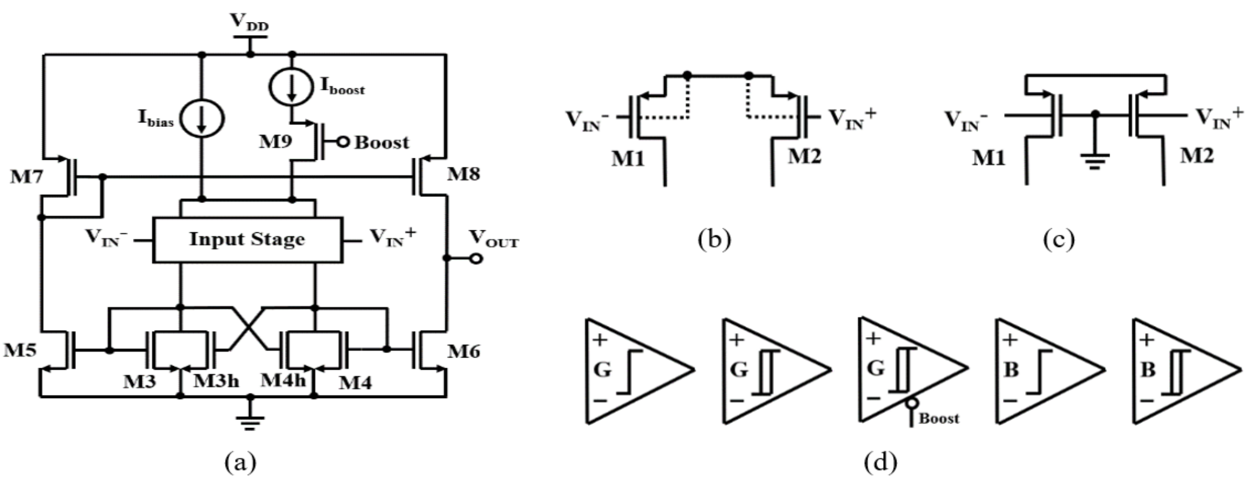


Figure 5. (a) Basic structure of the comparators (b) GD input stage (c) BD input stage (d) Comparator symbols (GD, GD with hysteresis, GD with hysteresis and boosting, BD, BD with hysteresis from the left).

The VD uses the comparator CMP2, which features hysteresis functionality and employs a body-driven input stage. The proposed interface circuit utilizes a total of 6 comparators, each with different structures and functions based on the required performance. The basic structure of the comparators is shown in Figure 5(a), where the input stage adopts either a gate-driven (GD) structure, as shown in Figure 5(b), or a body-driven (BD) structure, as illustrated in Figure 5(c). The GD structure is employed when a high input resistance and a substantial transconductance gain (g_m) under the given bias current are required. Conversely, the BD structure can be utilized when a wider input range is needed, even if the g_m is somewhat compromised. The hysteresis function is facilitated by M3h and M4h in Figure 5(a), where the width ratio of M3(=M4) and M3h(=M4h) determines the hysteresis width. If hysteresis function is unnecessary, omitting M3h and M4h suffices. If we need a boost in bias current, we include M9 and a current source (I_{boost}).

For the CMP1 in Figure 1, hysteresis functionality is necessary to achieve band-band control. Additionally, since it needs to compare the V_{MPPr} stored in a small capacitor, a high input resistance is required, leading to the use of the GD structure. In micro-energy harvesting systems, harvested energy is usually less than energy consumed by the load, making the EXP shorter than the ESP. During the rapid V_{BF} decrease in the EXP, CMP1 must operate faster to timely detect $V_{MPP,min}$. To achieve this, the bias current boosting feature in CMP1 is necessary.Figure 5(d) depicts the comparator symbols for various structures and functionalities. The bias generator is designed based on a beta-multiplier structure [20], providing around 0.4V V_{REF} and 5nA I_{REF} to the constituent blocks.

2.5. Rectifier (REC)

The REC is designed with a 2-stage structure consisting of a negative voltage converter (NVC) and an active diode (AD), as illustrated in Figure 6(a). The two-stage REC [6, 7] requires one more switch compared to the single-stage REC [2, 3, 11, 21] leading to an increase in conduction loss. However, due to the requirement of only one comparator, the static power consumption decreases. Therefore, in micro-energy harvesting systems, the two-stage REC may be more advantageous [22]. We designed the CMP3 and the buffer with a focus on minimizing current consumption to minimize the impact of the REC on the overall system efficiency. The designed CMP3 consumes a current of 110nA at a 3V supply voltage, exhibiting a gain of 69dB and a 3dB bandwidth of 40kHz. The transistor M_{SU} connected in parallel with SW4 is utilized for self-starting the system. Simulation results for the output power P_{REC} of the designed REC under f=100Hz and varying I_P are presented in Figure 6(b). The characteristics of the REC in week vibration conditions (f=15Hz, I_P=10µA) and strong vibration conditions (f=500Hz, I_P=666.5µA) are illustrated in Figure 6(c). Across various vibration environments, the designed REC generates power close to theoretical values. t can be observed that the designed REC generates power close to theoretical values across various vibration environments.

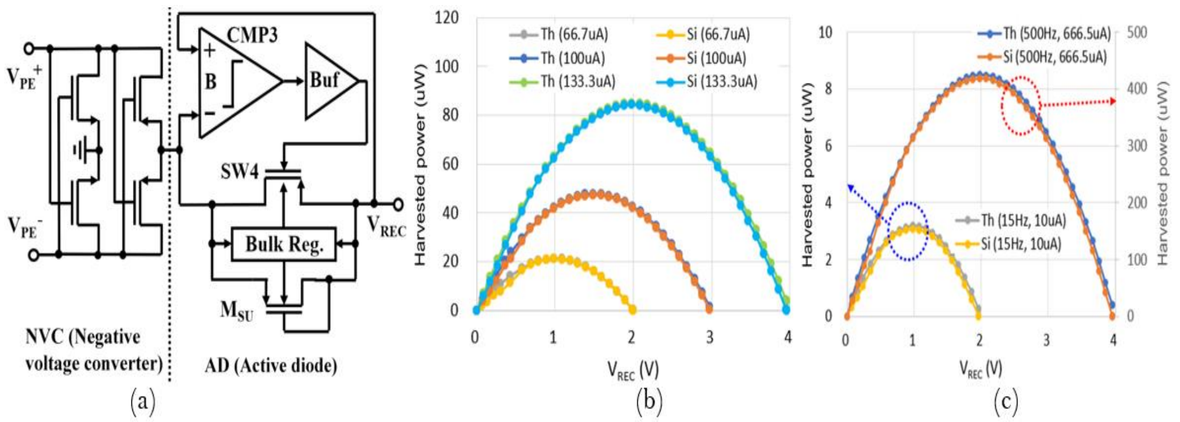


Figure 6. (a) Rectifier schematic (b) Simulated output power P_{REC} at different I_P (f=100Hz)(c) P_{REC} at f=15Hz, I_P=10µA and P_{REC} at f=500Hz, I_P=666.5uA (Th: theoretical, Si: simulated).

2.6. MPPT Controller

The proposed MPPT controller consists of four blocks: the MP generator (MPG), peak detector (PD), SP generator (SPG), and sample and hold (S/H), as depicted in Figure 7. Figures 8, 9, and 10 illustrate the simulation results of the constituent blocks for the cases of f=100Hz, I_P=100μA, and f_{MP}=1/32. In the MPG block, the CMP4 generates the clock signal CLK from V_{PE}^+, and the counter generates the MP signal at intervals set by the FS signal. As depicted in Figure 8, when the falling edge of the SP signal is detected, the D flip-flops are reset, causing the MP to go low, indicating the completion of the MTP. The PD operates on the MP_Psignal, a pulse with a rising edge that occurs half a clock cycle earlier than the MP signal.

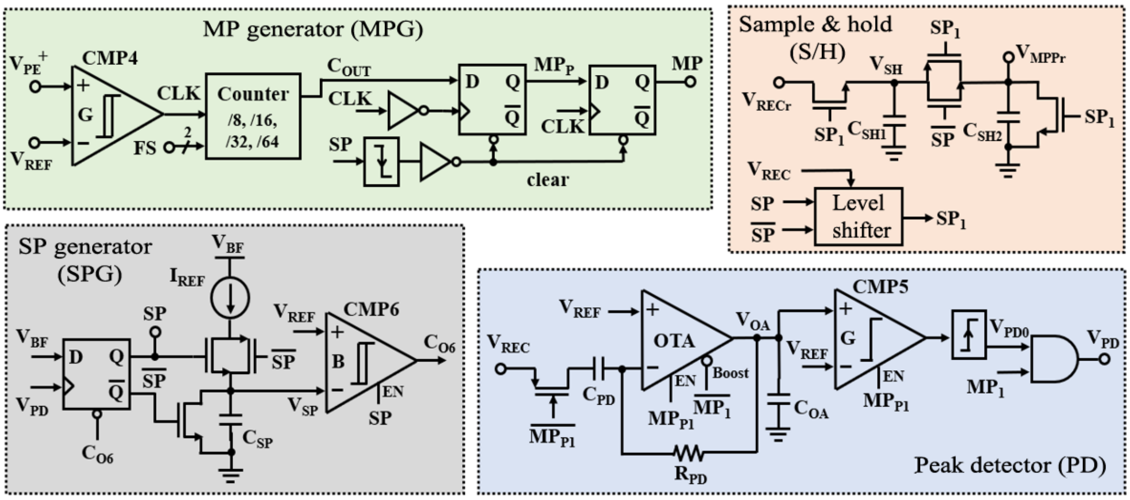


Figure 7. Simplified block diagram of the proposed MPPT controller.

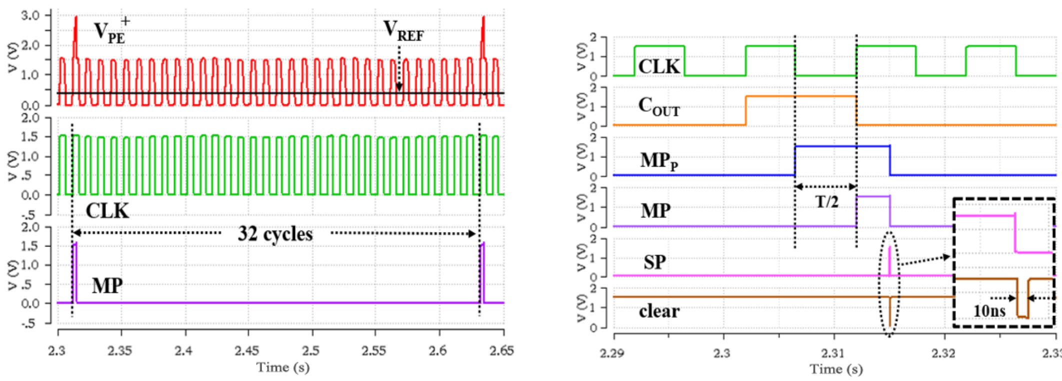


Figure 8. MPG simulation results.

The PD is composed of a differentiator consisting of an operational transconductance amplifier (OTA), C_{PD}, and R_{PD}, as well as a comparator CMP5. When V_{REC} reaches its peak, the PD generates a short-duration pulse, V_{PD}. The MP_1 and MP_{P1} used as enable signals or boost signals for the OTA and CMP5 are almost identical to the MP and MP_P generated in the MPG block. However, after the PD operation is completed, the falling edges of MP_1 and MP_{P1} are determined by V_{PD} instead of SP in order to immediately disable the OTA and CMP5. To minimize the current consumption, the OTA and CMP5 can be enabled only during MP_1. However, abruptly applying the enable signal can lead to transient responses, causing erroneous V_{PD} signals and potential malfunctions. Furthermore, at higher frequencies where the MP's pulse width reduces, proper operation can be challenging due to the time required for the transient responses to disappear.

In this paper, we employ the following technique to maximize the operational frequency: Instead of using MP_1 as the enable signal for the OTA and CMP5, the MP_{P1} whose rising edge occurs half a clock cycle earlier, is utilized. During the half a cycle, the transient conditions can stabilize, and the remaining time corresponding to

MP_1 is utilized for peak detection operations. To improve the performance of the differentiator, the OTA is bias-boosted during MP_1. It can be seen in Figure 9 that among the pulse signals of V_{PD0}, the pulse generated during MP_1 is finally selected as the correct V_{PD} signal.

When V_{PD} is generated, the SPG generates a pulse SP for V_{OC}sampling and V_{MPP} updating. By utilizing switches and a current source, it is possible to charge or discharge a small-sized capacitor C_{SP}, allowing the generation of a pulse with the desired pulse width. The conventional pulse generator that utilizes a Schmitt trigger [23, 24] is advantageous in terms of power consumption due to the absence of a comparator. However, it suffers from drawbacks such as relatively significant variation in pulse width with changes in the supply voltage and a delayed output. In Sanchez, et al. [6] a comparator is employed to achieve a more precise pulse width. However, using a resistor as a reference inevitably makes it sensitive to variations in process, voltage, and temperature (PVT). The SPG designed in this paper uses the V_{REF} generated from the bias generator as the reference voltage of the comparator, so it generates stabilized pulses that are less sensitive to PVT changes without delay. To reduce current consumption, the CMP6 is enabled only during the SP pulse duration. As shown in Figure 10, the designed SPG generates an SP signal with a pulse width of approximately 40µs immediately after the occurrence of V_{PD}.

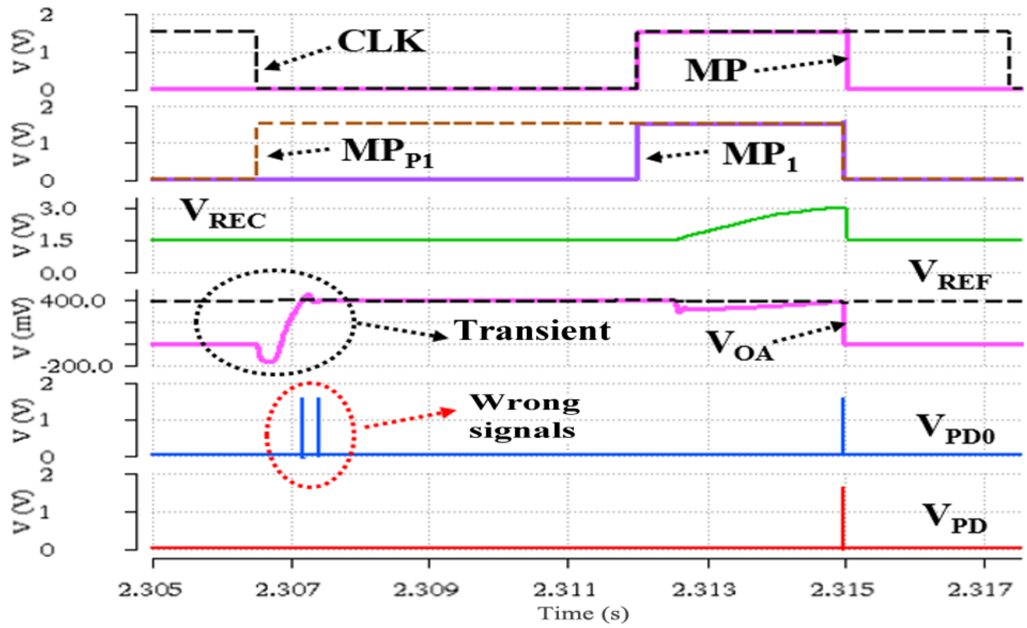


Figure 9. PD simulation results.

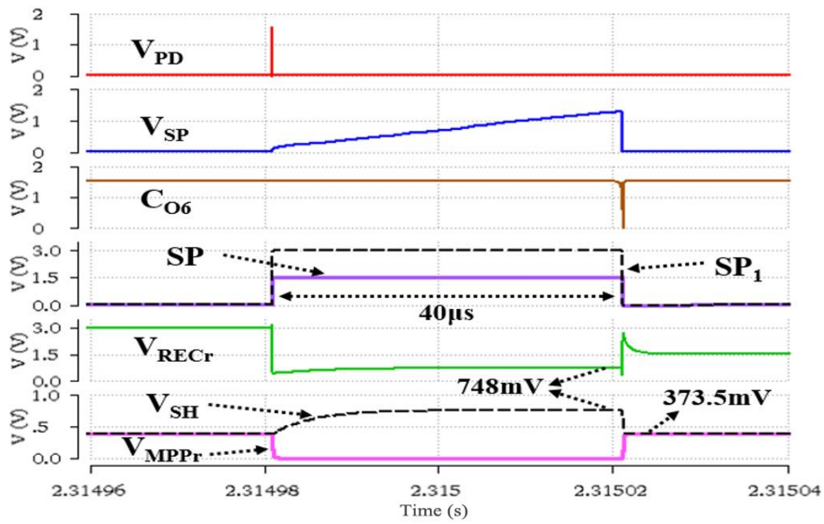


Figure 10. SPG and S/H simulation results.

In the S/H circuit, during the SP pulse duration, V_{RECr} (=V_{OC}/4) is sampled onto the 60pF capacitor C_{SH1}. At the same time, the charges previously stored in the identically sized C_{SH2} are discharged. When SP goes low, the charge stored in C_{SH1} is shared with C_{SH2}, resulting in the update of V_{MPPr} (=V_{MPP}/4), as depicted in Figure 10. During the SP pulse, V_{REC} becomes V_{OC}, so it is about twice as large as V_{BF}. Therefore, instead of SP, the SP_1 signal, whose high level is raised to V_{REC} using a level shifter [25] is used as the switch control signal. By using the SP_1 signal, it is possible to reduce the on-resistance of NMOS (N-type Metal Oxide Semiconductor) switches and enhance the off-resistance of PMOS (P-type Metal Oxide Semiconductor) switches. After the SP signal goes low, the V_{MPPr} is 373.5mV, exhibiting a small error of 1.9mV (0.51%) compared to the theoretical value of 375.4mV.

3. RESULTS AND DISCUSSION

Simulation results of the proposed circuit, designed using a 0.35µm CMOS process, are presented in Figure 11 for f=100Hz, I_P=100µA, f_{MP}=1/32, and R_L=10kΩ. The sizes of the off-chip devices, C_{REC} and C_{BF}, are 53nF and 47µF, respectively. After the start-up time (T_{SU}) of about 1.34s has passed since vibration occurs and the PEG starts operating, an EN signal is generated from the VD and the MPPT controller starts operating. It can be seen that V_{BF}, the output voltage of the PEG, is band-band controlled in a voltage range of 56mV relative to V_{MPP} as a reference. Moreover, the band-band control coincides with the occurrence of ESP and EXP. As R_L increases, the EXP region expands, and the time to supply power to the load, that is, the duty cycle of V_L, increases. The designed circuit consumes a current of 116nA when R_L=10kΩ and 94nA when R_L=1kΩ. This is because as R_L becomes smaller, the EXP region shrinks, and the time to supply boosting current to CMP1 decreases.

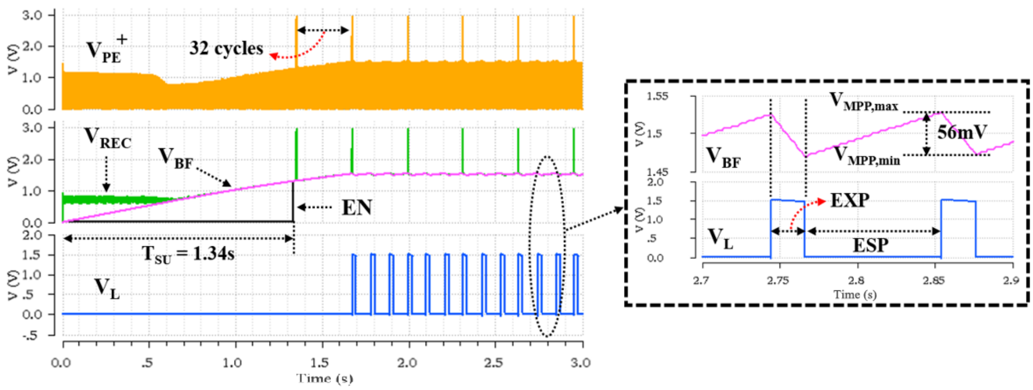
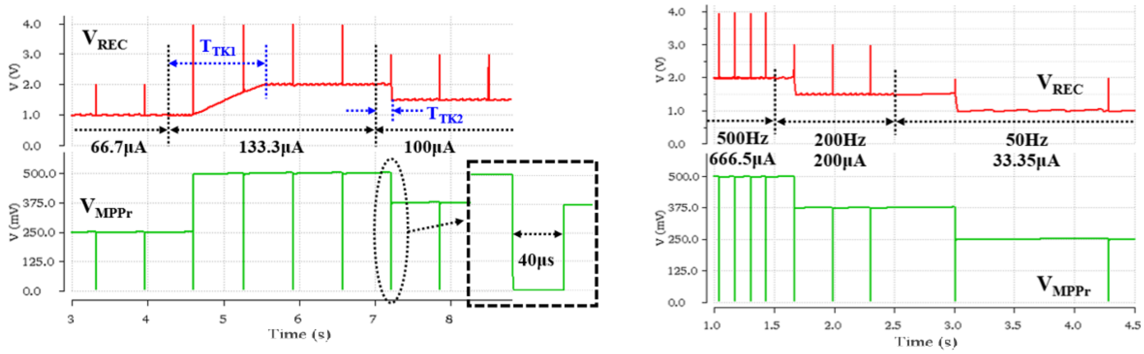


Figure 11. Overall simulation results (f=100Hz, I_P=100µA, f_{MP}=1/32, and R_L=10kΩ).

Simulation results illustrating the MPPT characteristics of the designed circuit under varying vibration conditions are presented in Figure 12. Figure 12(a) shows the simulation results under fixed vibration frequency f at 100Hz, where I_P varies from 66.7µA (V_{OC}=2V) to 133.3µA (V_{OC}=4V), and then to 100µA (V_{OC}=3V). Figure 12 (b) demonstrates the results when both f and I_P vary simultaneously, with each case corresponding to V_{OC} values of 4V, 3V, and 2V according to the test points in Table 2. When I_P changes, V_{MPPr} is updated in the following MTP, and it can be seen that V_{BF} (excluding the spikes in the V_{REC} waveform) approaches the new V_{MPP}. The tracking times, T_{TK1} and T_{TK2}, are 1.3s and 0.24s, respectively, indicating the time it takes for V_{BF} to reach the new V_{MPP} after a change in I_P. The tracking time is influenced by various factors such as vibration conditions (f, I_P), f_{MP}, R_L, and notably whether the change in vibration conditions occurs just before (best case) or immediately after (worst case) the MTP. When the new V_{MPP} is larger than the previous value, it becomes more influenced by the vibration conditions, and under strong vibration conditions, the boost-up time of V_{BF} decreases, leading to a reduction in T_{TK1}. Conversely, in the opposite scenario, the influence is on R_L, and lower values of R_L lead to a decrease in T_{TK2}.

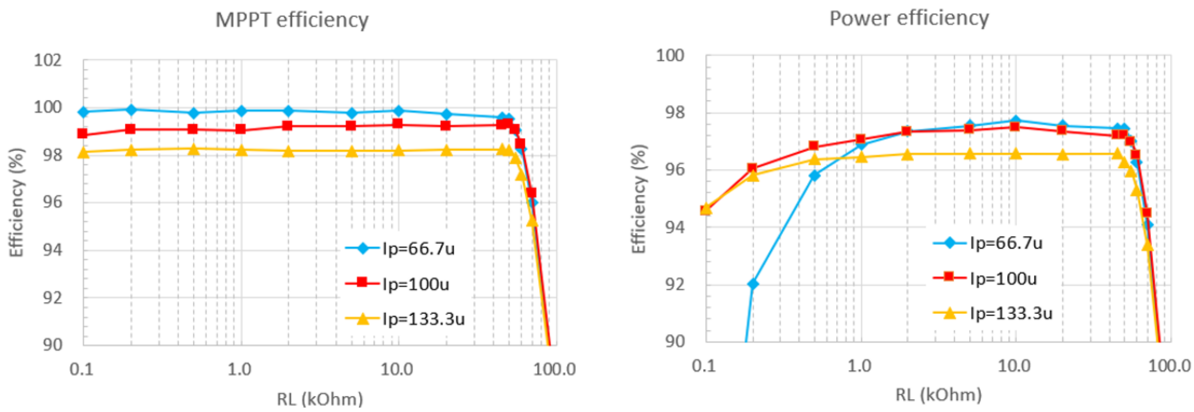
When f_{MP} is set to 1/64, MPPT efficiency and power efficiency according to R_L change and f change are shown in Figures 13 and 14, respectively. The MPPT efficiency is defined as the ratio between the power generated by the

PEH (P_{PEH}) and the theoretical maximum power (P_{max}) as given by (2). Power efficiency is defined as the ratio between the power supplied to the load (P_L) and P_{max}.



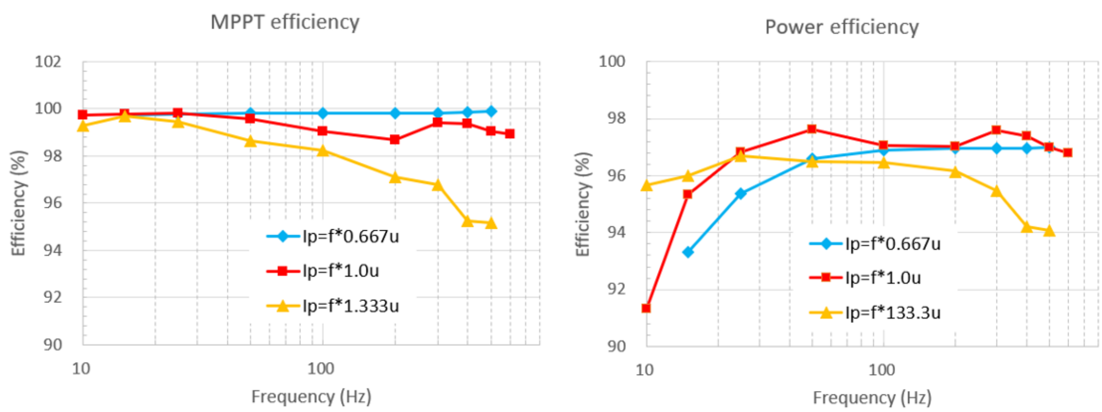
(a) (b)

Figure 12. MPPT characteristics (a) when f=100Hz and Ip changes (b) when both f and Ip change.



(a) (b)

Figure 13. (a) MPPT efficiency (b) Power efficiency at different R_L (f=100Hz).



(a) (b)

Figure 14. (a) MPPT efficiency (b) Power efficiency at different frequencies (R_L=1kΩ, * means multiply).

In Figure 13, when R_L becomes approximately 50 kΩ or higher, the duty cycle of V_L becomes 100%. At this time, because the power consumed by the load is less than the power harvested from the PEH, V_{BF} becomes larger than V_{MPP} and deviates from the MPP. Consequently, both MPPT efficiency and power efficiency decrease. In the range where the duty cycle is less than 100%, MPPT efficiency is over 98%, and the maximum value is 99.9%. Power efficiency is over 96% in the R_L range of 0.6kΩ or higher, and the maximum value is 97.7%. In the targeted V_{OC} range, when f_{MP} is fixed at 1/64, the designed circuit operates within a frequency range of 15 to 500Hz. Figure

14demonstrate that the MPPT efficiency and power efficiency in this frequency range exceed 95% and 93%, respectively. The designed circuit can supply up to 400µW of power to the load. By sacrificing current consumption to enhance the performance of the PD, it becomes possible to operate at higher frequencies. Additionally, adjusting the FS configuration to increase f_{MP} allows operation at even lower frequencies.

Table 3 summarizes the performance of the designed circuit. Compared to FBR-type interface circuits using the existing FOCV technique, the V_{OC} sampling time of the proposed circuit is less than half cycle, and the MP duty cycle is reduced by more than 3.7 times. As a result, the additional power loss required for MPPT can be minimized. It can also operate over a wider frequency range and consume much less current. The maximum power efficiency and maximum MPPT efficiency are 97.7% and 99.9%, respectively, demonstrating excellent performance.

Table 3. Performance comparison with conventional piezoelectric energy harvesting interfaces.

Parameters	This work	Lu, et al. [11]	Shim, et al. [2]	Yu [3]	Chew and Zhu [4]	Sanchez, et al. [6]	Li, et al. [7]
Process	0.35µm CMOS	0.35µm CMOS	0.35µm BCDMOS	0.35µm CMOS	Off-chip	0.35µm CMOS	0.13µm CMOS
Rectifier scheme	FBR	FBR	FBR	FBR	FBR	Parallel-SSHI	Parallel-SSHI
Rectifier type	2-stage AD	1-stage AD	1-stage AD	1-stage AD	Diode bridge	2-stage AD	2-stage AD
DC-DC converter	None	None	Buck-boost	Boost	Buck	Buck	Buck-boost
Input voltage (V_{OC})	2~4V	~6.5V	1~7V	2.5~5V	21~34V	N/R	1.6~4V
Output voltage	1V~	1.8V~	1~8V	3V	1.8~3.8V	0.7V~5V	1.2~3.3V
Operation frequency (Hz)	~500	~200	N/R	~200	2~10	134.6~229.6	100~180
MPPT	Yes	Yes	Yes	Yes	Yes	No	Yes
MPPT algorithm	FOCV	FOCV	FOCV	FOCV	Direct FOCV	N/A	P&O
MP frequency	Adjustable	1/128	1/50	1/128	N/A	N/A	N/A
MP duty cycle (%)	0.42 (@1/64)	1.56	2.0	1.56	N/A	N/A	N/A
V_{OC} sampling time	< 1/2 cycle	2 cycles	1 cycle	2 cycles	N/A	N/A	N/A
Maximum power efficiency (%)	97.7	96	80 (Just DC-DC)	83.4	N/R	96.6	78 (Just DC-DC)
Maximum MPPT efficiency (%)	99.9	98.3	99	99	98.28	N/A	97
Output power	~400µW	~261µW	N/R	N/R	~2.4mW	~420µW	~330µW
Current consumption	94nA[a]	N/R	10µW (@2.7V)	N/R	5.16~6.78µW	N/R	1.57µA

Note: a: f =100Hz, I_P =100µA, R_L =1kΩ. N/R: Not reported. N/A: Not applicable. BCDMOS: Bipolar CMOS DMOS. P&O: Perturb and observe.

4. CONCLUSION

This paper presents a piezoelectric energy harvesting interface with fast V_{OC} sampling using an adaptive tracking pulse. Since the duty cycle of the tracking pulse is very small at 0.42%, it is possible to improve power efficiency by 1.14% and 2.71%, respectively, compared to the case of using the 1-cycle or 2-cycle fixed pulse. Additionally, the appropriate control of the enable signals supplied to peak detector expands the operable frequency range. The proposed circuit, designed with the 0.35um CMOS process, can supply up to 400µW to the load in the

V_{OC} range of 2~4V and the frequency range of 15~500Hz, and the maximum MPPT efficiency and maximum power efficiency are respectively 99.9% and 97.7%. The proposed interface can operate across a wide frequency range and input voltage range, making it applicable for various applications.

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Transparency: The authors state that the manuscript is honest, truthful, and transparent, that no key aspects of the investigation have been omitted, and that any differences from the study as planned have been clarified. This study followed all writing ethics.
Competing Interests: The authors declare that they have no competing interests.
Authors' Contributions: Both authors contributed equally to the conception and design of the study. Both authors have read and agreed to the published version of the manuscript.

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